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ENEE 244 Digital Logic Design, Summer 2008

(Section 101; CHE2145; MTWTh 9:30 – 10:50 a.m.)

Course Objective: To gain understanding of and skill at doing logic design of digital systems.
Text: Donald D. Givone, *Digital Principles and Design*, McGraw-Hill, 2002, ISBN: 0-07-252503-7.
Required Materials: MIL-STD806C Logic Symbol Template, Halfsize, (e.g., Pickett 1222, Rapid Design RPD-R-542, or eqivalent).

Grading:		
Exam I	(about class 13: Mon., June 23)	30%
Exam II	(about class 24: Thurs., July 10)	30%
Final Exam	(firm date: Wed., July 23)	30%
Homework, unannounced quizzes, & instructor's subjective impression of class participation		10%

Exams are **closed book, closed notes & no electronic devices such as calculators, PDAs, etc.***; Homework will be collected & marked.* Letter grades are based on higher of raw or scaled semester average: A $\geq$ 90%, 80% $\leq$ B $\leq$ 89%, 70% $\leq$ C $\leq$ 79%, 60% $\leq$ D $\leq$ 69%, F $<$ 60%.

- If your final exam score is higher than your lowest score on Exam I or Exam II, then the final exam score will replace that lowest score in computation of your semester average.
- **No makeup exams will be given for any reason.** If you must miss an exam, you must first get permission from Professor Silio before the exam, and the final exam score will count for that portion of the grade. This will count as your one replacement.

Topical Outline: (Subject to revision by instructor) (Ch. = Chapter, S = Section(s))

1. Binary Numbers; binary arithmetic and codes (Ch. 2, S: 2.1–2.11)
2. Boolean Algebra, switching algebra, and logic gates (Ch. 3, S:3.1–3.8, & Silio Notes)
3. Karnaugh Maps, simplification of Boolean functions (Ch. 4, S: 4.1–4.7)
4. Combinational Design/Analysis; two level NAND/NOR implementation; & multilevel NAND/NOR/XOR circuits (Ch. 3, S: 3.9–3.10)
5. Tabular Minimization (Quine McCluskey) (Ch. 4, S: 4.8–4.9, 4.9.2, 4.10–4.13.3, 4.13.5–4.13.6)
6. Exam I (Exact date will be announced in class.)
7. Adders, subtracters, BCD adders, code converters, parity checkers. (Ch. 5, S: 5.1–5.2)
8. MSI Components, design and use of comparators, encoders, decoders, & multiplexers (Ch. 5, S: 5.3–5.6.1)
9. Latches and flip-flops (Ch. 6, S: 6.1–6.6)
10. Synchronous sequential circuit design & analysis (Ch. 7, S: 7.1–7.3 & 7.6)
11. Registers, synchronous and asynchronous counters (Ch. 6, S: 6.7–6.9)
12. Exam II (Exact date will be announced in class.)
13. Programmable Logic, ROMs, PLDs, PLAs, PALs (Ch. 5, S: 5.7–5.10 & Ch.7, S: 7.6.1)
14. Wired logic and characteristics of logic gate families (Appx. A, S: A.1, A.3–A.5, A.7–A.11)
15. Final Exam (Firm date; see "Grading" section above.)

Optional Topics as time permits:

1. State Reduction and Good State Variable Assignments (Ch. 7, S: 7.4–7.5)
2. Algorithmic State Machine (ASM) Charts (Ch. 8)
3. Asynchronous sequential circuits (Ch. 9)

Office Hours: Mon., Tues, Wed., & Thurs.: 11 a.m. – 12 noon
in room number: **AVW-1329** **Other times by appointment.**

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- If you have problems with my office hours you can make an apointment. My phone number is 301-405-3668, and my home number is 301-937-7418 in case you need to reach me.
- If you have a **documented disability** and wish to discuss academic accommodations with me, please contact me as soon as possible and **not later than Tuesday, June 10**.
- If **any exam** (especially the final exam) is scheduled on a **religious holiday** that you are compelled to observe, and you must make arrangements to take the exam on a different date, please see me about making these arrangements **not later than Tues., June 10**.

Homework and Grading Policies

- There will be approximately 11–12 homework assignments during the semester. Homework is due at the **beginning** of class on the date indicated. **No late homework will be accepted for any reason.**
- Do homework on 8.5×11 inch paper with problems in the order of assignment. **Label the first page in the upper right hand corner with your full name, course number (ENEE244), and homework assignment number.** Staple the pages in the upper left-hand corner, and do not fold them.
- If you dispute your grade on any homework or exam, you have one week from the date the paper was returned to request a change in grade. After this time, no change in grade will be considered. All requests for a change in grade must be submitted in writing. A request for change in grade must be labeled in the same manner as a homework assignment with name and course number.
- It is important that you do the homework in order to understand the material in the course. While it is reasonable to discuss your approach to solving the problems with a friend, the final writeup of the solution should be your own work and not a copy of your friend's.
- Typically, graded homeworks will be returned one week after they are collected. Since it is not possible in finite time for the grader to mark all assigned problems in detail, solutions will be made available for each homework assignment and you should go over them in detail yourself to correct any errors you may have made that were not caught in the marking process. Therefore, to avoid delays you might want to retain a photocopy of your homework solutions both to do this and to study for exams.
- It is your responsibility to pick up handouts, solutions, and homework assignments when they are passed out in class. Professor Silio will not retain copies after the class in which the handout is passed out. If you must miss class, make arrangements with a reliable classmate to pick up a copy of the handout material for you; or make arrangements with other classmates to photocopy theirs.
- A **course ftp web site** will be maintained in AFS directory:
  /afs/glue/department/enee/public_html/class/enee244-1.Sum2008,
  (URL **http://www.ece.umd.edu/class/enee244-1** under
  Summer 2008), which contains information, Notes and Homework. If you miss class, you may be able to find the missed handout here in either postscript or pdf format.

Reminder about Academic Integrity

- Academic dishonesty will not be tolerated. The University Code of Academic Integrity, which can be found at http://www.inform.umd.edu/CampusInfo/Departments/JPO/
  prohibits students from committing the following acts of academic dishonesty: cheating, fabrication, facilitating academic dishonesty, and plagiarism. Academic dishonesty in this class includes outright copying on homework; however, discussing homework problems and exchanging tips is permissible and also encouraged. If there are any take-home exams, discussing the material with anyone other than privately with the instructor, inside or outside of the class, is considered academic dishonesty. Instances of academic dishonesty will be referred to the Office of Judicial Programs.

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Recommended Study Habits

- Read the specified sections of the book before class.
- Attend lecture and take written notes.
- After lecture recopy your notes, and study the reading assignment.
- Start on the homework problems early and take advantage of office hours.
- Do not fall behind!
- This course requires 3 hours of work (reading, doing homework, and reviewing for exams) per lecture hour; so you can expect to be devoting 22 to 25 hours per week to this class (including class lecture time).

Additional References

- M. Morris Mano, *Digital Design, 3rd Edition*, Prentice Hall, 2001, ISBN: 0-13-062121-8.
- M. Morris Mano, *Digital Design, 2nd Edition*, Prentice Hall, 1991, ISBN: 0-13-212937.-X.
- A. B. Marcovitz, *Intro. to Logic Design, 2nd Edition*, McGraw-Hill, 2005, ISBN: 0-07-295176-1.
- V. P. Nelson, H. T. Nagle, B. D. Carroll, J. D. Irwin, *Digital Logic Circuit Analysis & Design*, Prentice-Hall, 1995, ISBN: 0-13-463894-8.
- John P. Hayes, *Intro. to Digital Logic Design*, Addison-Wesley, 1993, ISBN: 0-201-15461-7.
- Stephen Brown & Zvonko Vranesic, *Fundamentals of Digital Logic with VHDL Design*, McGraw-Hill, 2000, ISBN: 0-07-012591-0.
- Stephen Brown & Zvonko Vranesic, *Fundamentals of Digital Logic with Verilog Design*, McGraw-Hill, 2003, ISBN: 0-07-282315-1.
- R. H. Katz and G. Borriello, *Contemporary Logic Design, 2nd Ed.*, Pearson Prentice Hall, 2005, ISBN: 0-201-30857-6.
- Charles Roth, Jr., *Fundamentals of Logic Design, 5th Ed.*, Brooks/Colle Thomson Learning, 2004, ISBN: 0-534-37804-8.
- Z. Kohavi, *Switching and Finite Automata Theory, 2nd Ed.*, McGraw-Hill, 1978, ISBN: 0-07-035310-7.