Electrical and Computer Engineering Department University of Maryland

College Park, MD 20742-3285

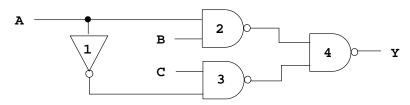
Glenn L. Martin Institute of Technology ♦ A. James Clark School of Engineering Dr. Charles B. Silio, Jr.

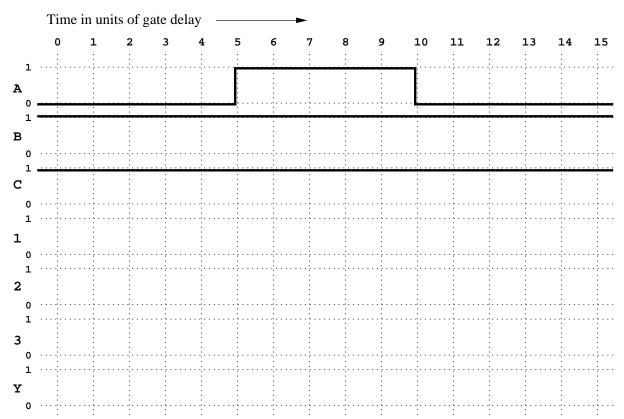
ENEE 244 Homework Set 10

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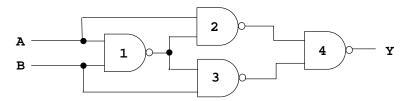
(Due: Mon., Apr. 21, immediately preceding Class 23, Tues., Apr. 22, 2014) silio@umd.edu

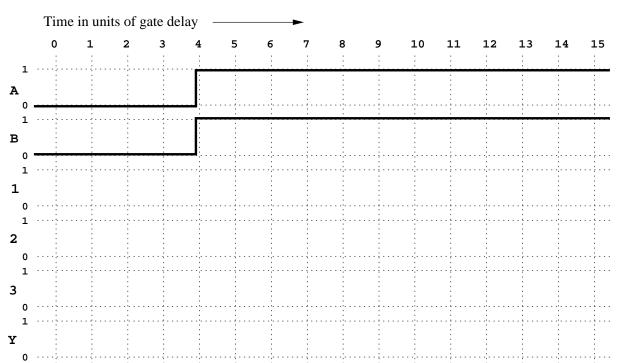
1. Assume the gate propagation delay for each gate is 1 time unit, and draw the timing diagram for all of the gate outputs in response to the input signals (A, B, C) shown.



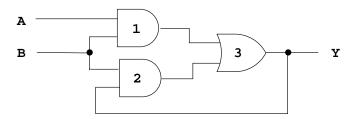


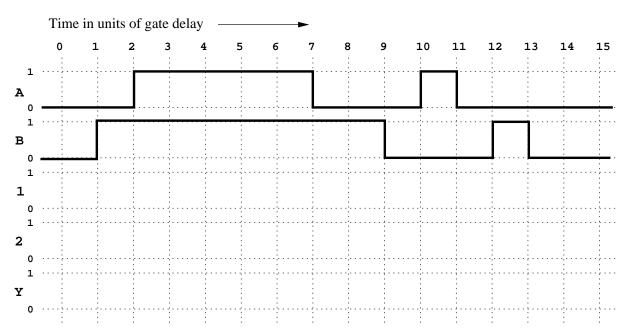
2. Assume the gate propagation delay for each gate is 1 time unit, and draw the timing diagram for all of the gate outputs in response to the input signals (A and B) shown.





3. Assume the gate propagation delay for each gate is 1 time unit, and draw the timing diagram for all of the gate outputs in response to the input signals (A and B) shown. Assume A(t) = B(t) = 0, t < 0.





Read all of Section 6.8 of Givone and read Sections 7.3.3–7.5.2; then work the following problems:

- 4. Prob. 6.22.
- 5. Prob. 6.23.
- 6. Prob. 6.27.
- 7. Prob. 6.28.
- 8. Prob. 6.30.
- 9. Prob. 7.7.
- 10. Prob. 7.12.