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ENEE 244 Homework Set 12
(Due: Class 29, Tues., May 13, 2014)

1. Read Givone Sections 9.9.1–9.9.5 and the introduction section 9.9 on Static and Dynamic Hazards, pp. 561–571. debounce a mechanical switch.

2. Now we will delve into the next abstraction level down from logic gates into how they are implemented using transistors (at least to obtain a seat of the pants view so as to not fear their appearance in data sheets). Remember in the following reading assignment our goal is not to reproduce voltage, current calculations; read them (your knowledge of electricity from physics should be enough to get you through) but don't get stuck on the equations or calculations; the descriptive material on how and why things work is more important. This is a brief introduction and you may not understand all of it at first glance (this is not an electronics course where you will need to know these things in detail, but that comes in another course later). There are a few things that you should pay attention to and that logic designers should know. So read Textbook Appendix A Sections A.1, A.3–A.5, & A.7–A.11 and concentrate especially on the topics:

   a. open collector gates and wired logic

   b. tri-state (three state) gates

   c. fan-in/fan-out

   d. propagation delay

   e. noise margins

3. Look over the handout on how to implement an XOR gate with transmission gates (one p-mos and one n-mos transistor in parallel with some inverters) and look at the CMOS tri-state inverter and buffer amplifier so as to explain (from the logic viewpoint) how they work.