State Machines

ENEE 245: Digital Circuits and Systems Laboratory, Fall 2014
Lab 3

Objectives

The objectives of this laboratory are the following:

- To design a simple state machine
- To test the state machine on various inputs

State machines are the fundamental underpinnings of computers and computer systems. In this lab, you will build a simple 2-bit saturating counter and test it manually.

A saturating counter is one that does not "wrap around" when it reaches the maximum or minimum value. In normal 2's complement arithmetic, when a binary number reaches the maximum possible value and you add 1 to it, you get the largest negative number as a result. Similarly, when you subtract 1 from the minimum number you get the largest positive number as a result. This can be seen in a simple 3-bit example:

```
011   3
010   2
001   1
000   0
111   -1
110   -2
101   -3
100   -4
```

If you add 1 to the binary value "011" you get "100" which, in a 4-bit representation or larger, would equal the decimal number 4. However, in a 3-bit number, this is the value -4. Similarly, if you subtract 1 from the binary value "100" you get "011." This is normal behavior in 2's complement.

Saturating counters are those that do not wrap around. If you add 1 to the largest positive number in a saturating counter, the counter stays pegged at that number. If you subtract 1 from the largest negative number, the counter stays pegged there as well.

Pre-Lab Preparation

Design a 2-bit saturating counter using any of the following components:

- a 4-bit clocked register
- a 2-bit adder
- multiplexers (2-to-1 and/or 4-to-1)
- individual NAND gates, NOR gates, and/or inverters

You do not have to design the internals of the components, as you have already done that in the previous two labs. Your counter should increment when it receives a "1" as input, decrement when it receives a "0" as input, and hold at maximum & minimum values of "01" (decimal 1) and "10" (decimal -2).

Draw the logic diagram as well as the wiring diagram using the available CMOS chips.

Use SPICE to simulate your design, using a clock input (alternating 0/1 values) at all four starting points of the counter, with both possible starting points of the clock. In other words, run eight

different SPICE simulations. Most importantly are the "01" counter starting point with a "1" input value from the clock to begin with and the "10" counter starting point with a "0" input value from the clock to begin with. Hopefully the reason why these are the most important test cases is clear.

Think about how you are going to use the DLA to do the same sort of testing as SPICE simulation.

In-Lab Procedure

Bring flash drives to store your traces.

Ask the TA questions regarding any procedures about which you are uncertain.

Turn off all power supplies any time that you make any change to the circuit.

Do NOT apply more than 5 V to the circuit at any time.

Arrange your circuit components neatly and in a logical order.

Compare your breadboard carefully with your circuit diagram before applying power to the circuit.

Complete the following tasks:

- Construct your 2-bit saturating counter.
- Drive your counter with a 1-second clock, a 7-segment display, and a manual "1/0" add/sub control input.
- Manually test your counter to reach all possible combinations of counter values and input values.
- Record the full test through the logic analyzer to show that all possible combinations of state and input were tested.

Post-Lab Report

Write up your circuit, schematic, and lab procedure. Demonstrate the correctness of your design using the test results that you collected in the lab.