
# MOSFETs and Voltage Boosting

**ENEE 245: Digital Circuits and Systems Laboratory**
**Lab 4**

## Objectives

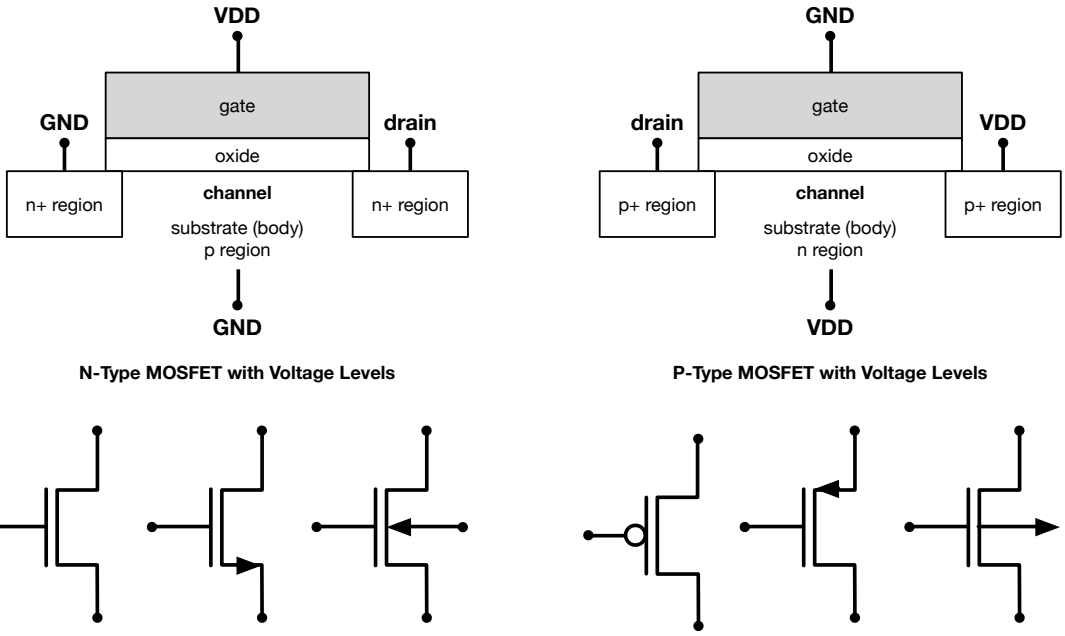
This laboratory is a brief introduction to MOSFETs. The objectives of the lab are the following:

- To see MOSFETs in action and to begin to understand their behavior
- To understand some of the significant limitations of MOSFETs
- To see how voltages are boosted in modern digital ICs

This lab will focus more on experimentation and measurement than on circuit design. The purpose is to make you aware of certain transistor characteristics and techniques in the field of digital design.

## MOSFETs

Underlying all digital circuits today are *metal-oxide-semiconductor field-effect transistors*, or *MOSFETs* for short. These are little switches that can either conduct or not conduct current, given the presence or absence of voltage on a control signal. There are two main types, n-type and p-type, depending on what material they are built in, and they have the following symbols and behaviors:

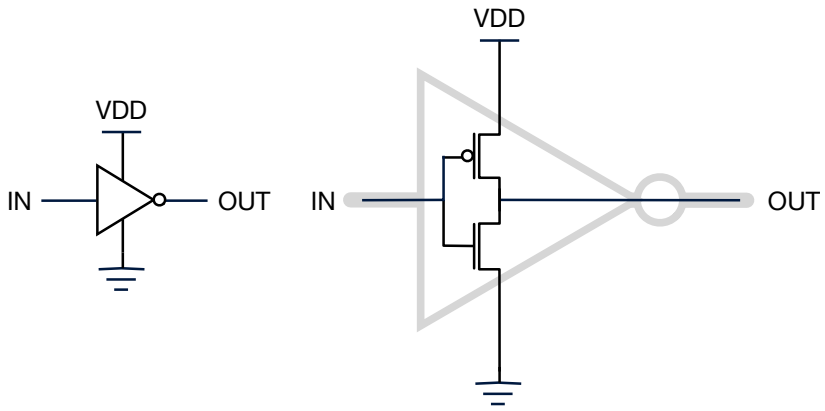



*MOSFETs in silicon (top) and several of their symbolic forms used in digital electronics (bottom)*

You will notice that, as drawn at the top, they are 4-terminal devices (gate at the top, source and drain at the sides, and body or bulk at the bottom), but when they are drawn in schematic form, they frequently are shown as 3-terminal devices (the most commonly appearing symbol is the leftmost symbol, followed by the middle symbol). They are shown as 3-terminal devices for simplicity when the body terminal is assumed to be as shown in the topmost figures above. In other

words, if an n-type MOSFET is used with its body tied to GND, the schematic will typically not bother showing that explicitly. When the body is tied to something other than the typical value, the fourth terminal should be shown explicitly. Also, with regards to the middle symbols above, which are identical other than a small arrow either pointing toward or away from the gate, the convention is that these symbols are always drawn vertically like this, and the arrow is on the side of the source (the side closest to the power rail—for p-type FETs, the side closest to VDD; for n-type FETs, the side closest to GND), and the symbols indicate direction of current, which is by convention from top of the schematic to the bottom of the schematic. So it would be weird to attempt to show an n-type FET with the arrow on the top side, pointing away from the gate.

Anyway, the main point is that MOSFETs are switches, and they feature prominently in the design of all modern digital ICs (integrated circuits). For instance, the most fundamental digital circuit is the CMOS inverter, which uses a pair of MOSFETs connected with their gates and drains tied together as follows:




*Inverter as symbol (left) and CMOS implementation (right)*

When the input voltage is high enough (i.e., close enough to logical "1"), the voltage level shuts off the p-type FET (on the top) and turns on the n-type FET (on the bottom), thereby connecting the output to GND (which is logical "0"). When the input voltage is low enough (close enough to logical "0"), the voltage level shuts off the n-type FET (on the bottom) and turns on the p-type FET (on the top), thereby connecting the output to VDD (logical "1"). Ergo: inverter. The interesting thing about this circuit (and all of CMOS, in fact) is that the signal itself is not inverted or even changed at all: it is used to control the FETs such that, through them, the output is connected directly to either VDD or GND. Effectively, they are used as signal repeaters in this regard.

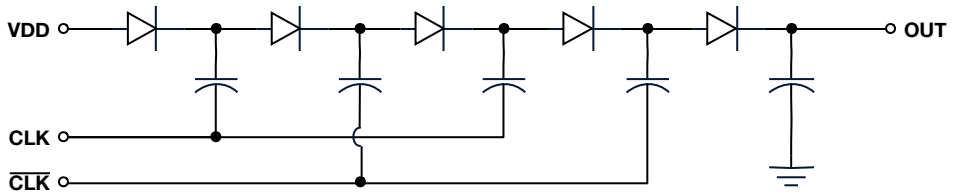
However, note that, even though we use these devices to implement digital circuits, they really do have analog behavior. For example, when the input voltage to the inverter above is in the middle of GND and VDD, both MOSFETs are partially on (neither is fully turned off), and the output voltage is somewhere between VDD and GND.

## High Voltage Boosting

In modern digital chips, there are many scenarios in which the on-chip voltage needs to be boosted to a higher level. For example, one of the ways in which MOSFETs are used as analog components in digital systems is as *pass transistors*—i.e., to pass an analog voltage from one place to another, for example from a storage cell to a sense amplifier. As you will see, the voltage that gets passed is no higher than the gate voltage, and it is often lower than that (depends on the MOSFET and voltage level). So to pass a given voltage, one might have to use a slightly higher voltage.

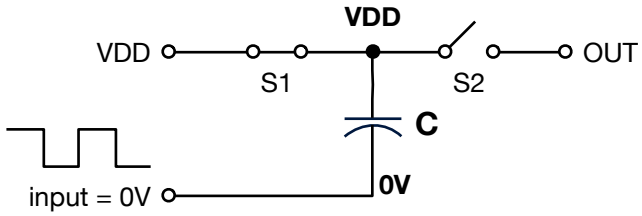
On memory chips such as DRAM, NAND/NOR Flash, Phase Change Memory, etc., there are many different voltages coursing around the chip at different times. These voltages are needed for the chip to perform various operations: for example, flash chips require large negative/positive voltages to erase/write the cells (usually 10–20V), and they require voltages around 5V to read the cells. These higher voltage levels must be present whether the chip is connected to a 110/220V wall outlet or in a cellphone powered by a 1.8V battery.

It should be clear that on-chip voltage boosting is important. It is widely used, and it is a staple of digital integrated circuits, so it is valuable for you to see it in action. One of the first example circuits that engineers see in school is the Dickson charge pump:

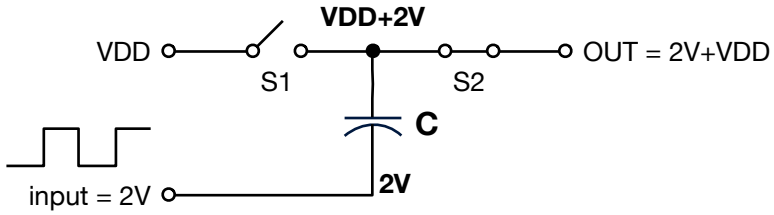



*Four-stage Dickson charge pump*

The main principle behind this, the main principle of voltage boosting, is that, unless discharged, a capacitor's charge is conserved—and this is true even when one of its terminals is switched to a different potential. When one terminal is raised, so is the other. Consider the figure below. In phase 1, at the top, switch S1 is closed, and the input (for instance an oscillating signal swinging 0V–2V) is in its "low" phase, putting GND at the bottom plate of capacitor C. The capacitor is charged to VDD by the power supply through switch S1. Switch S2 is open, preventing the capacitor from discharging. In phase 2, switches S1 and S2 have changed orientation, and the oscillating input is in its "high" phase, during which it is equal to 2V. Now, the top plate of capacitor C is connected to the output, and the bottom plate of capacitor C is connected to 2V (the clock's "high" value). Due to charge conservation, there must remain a potential of VDD across the capacitor, and so the top plate must assume a potential of VDD on top of 2V, or 2V+VDD, relative to GND.



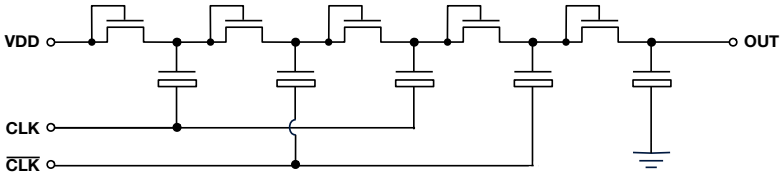

***Phase 1: Bottom plate of capacitor C given potential of GND; Capacitor C charged to VDD; Input swings 0V–2V***




***Phase 2: Bottom plate of capacitor C given potential of +2V Voltage drop across capacitor must remain VDD; Top plate goes to 2V+VDD***

*Principle of voltage boosting illustrated*

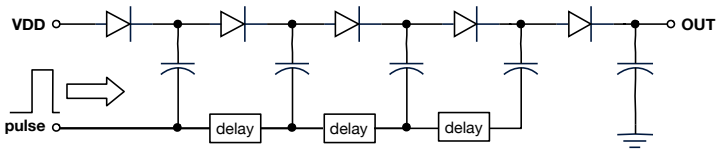
In integrated circuits, transistors are used to create both the diodes and the capacitors of the charge pump, and so the Dickson charge pump from earlier is wired as follows in a typical IC:




*Four-stage Dickson charge pump as wired in an integrated circuit*

Note that each of the components is really a MOSFET wired in the appropriate way: MOSFETs with their gates tied to their source terminal are *de facto* diodes; MOSFETs with their source and drain (and/or body) tied together are *de facto* capacitors. This type of charge-pump design is very common in CMOS circuit designs for precisely this reason.

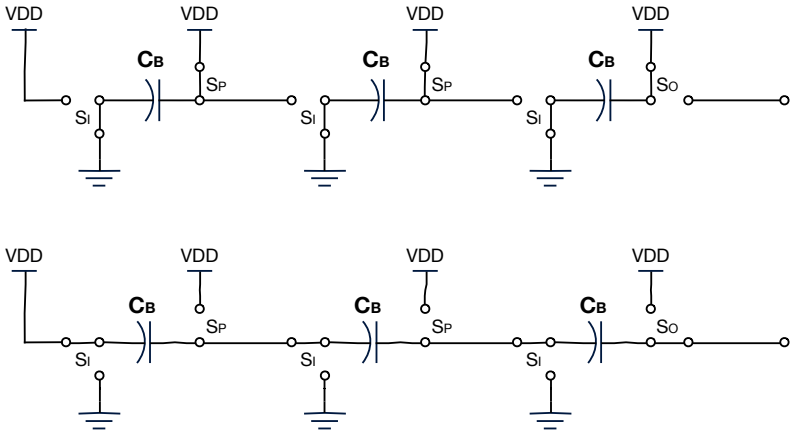
You can also send simple pulses through these circuits. For example, if an application requires a higher voltage than 2*VDD, but for only a short period of time, it would be possible to extend the earlier single-pulse example to a multi-stage pump. This amounts to the figure below.




*Multi-stage charge pump timed with a single pulse*

Provided that each stage's timing pulse does not overlap with that of the previous stage, this provides a one-time voltage boost on the output similar to a single cycle output of the continuously operational pumps above. Inserting delays in the signal chain enforces this requirement.

One issue of on-chip voltage boosting is that, as input voltage supplies get lower (e.g., battery-driven ICs running at 1.8V or lower), the diode drops become increasingly significant … each pass through one of the diodes above is on the order of a half a volt, rendering the Dickson charge pump less than ideal for low-voltage applications. A better design for such applications is the heap charge pump which has become popular in flash memories, as shown below:




*Heap charge pump — general principle of operation: charge phase (top), boost phase (bottom)*

The main differentiator in the heap charge pump is that, during the boost phase, the capacitors are wired in series and therefore require no diodes to prevent backflush. This reduces the overhead of boosting, enabling a larger boost with fewer losses; due to this, the heap charge pump is, at least potentially, a better solution for low-VDD applications.

## Pre-Lab Preparation

In this lab you will do two things, which should teach you a bit about MOSFETs and on-chip voltage boosting:

- You will develop a plot that shows, for various input voltages and gate voltages, what voltage is passed through an n-type MOSFET.
- You will build a 2-stage Dickson charge pump out of discrete parts and MOSFETs.

This lab will thus be primarily experimental, with a reduced emphasis on design. You must do the following for preparation:

- Develop a breadboard wiring diagram for the capacitor- and diode-based charge pump.
- Develop a breadboard wiring diagram for the 2-stage (not 4-stage) charge pump, using the capacitors and MOSFETs described in the next section.
- Print or draw several copies of a 10-by-10 grid for the MOSFET measurements.

Remember to bring two copies of your pre-lab write-up: one for you and one for the TA.

## In-Lab Procedures

*Part One: MOSFET Characterization*

You will use a three-terminal n-type MOSFET, which has the source and body tied together. This is the 2N7000 transistor, and the data sheet is on the course website. Connect the drain to a voltmeter probe and a 1K resistor to ground. Apply 0V–10V to the gate, in 1V increments, and 0V–10V to the source, in 1V increments, and record the output at the probe. You should see some unexpected behaviors. In general, to get a certain voltage passed through the MOSFET, what voltage must you put at the gate?

*Part Two: Charge Pump Operation*

Wire up the two-stage Dickson charge pump using discrete capacitors and diodes. Record the clock input and resulting voltage output. Now replace the discrete components with MOSFETs wired as diodes and capacitors. What difference do you see? What can you conclude?

*Reminders*

Bring flash drives to store your traces.

Ask the TA questions regarding any procedures about which you are uncertain.

Turn off all power supplies any time that you make any change to the circuit.

Do NOT apply more than 15V to the circuit at any time.

Compare your breadboard carefully with your circuit diagram before applying power to the circuit.

## Post-Lab Report

Write up your lab procedure and results, answering the questions posed in the write-up above.