power remains on. Dynamic RAMs, on the other hand, must be refreshed periodically to compensate for leakage from the little capacitors on the chip.

The components of a computer system are connected by buses. Many, but not all, of the pins on a typical CPU chip directly drive one bus line. The bus lines can be divided into address, data, and control lines. Synchronous buses are driven by a master clock. Asynchronous buses use full handshaking to synchronize the slave to the master.

The Pentium 4 is an example of a modern CPU. Modern systems using it have a memory bus, a PCI bus, an ISA bus, and a USB bus. The PCI bus can transfer 64 bits at a time at a rate of 66 MHz, which makes it fast enough for nearly all peripherals, but not fast enough for memory.

Switches, lights, printers, and many other I/O devices can be interfaced to computers using parallel I/O chips such as the 8255A. These chips can be configured to be part of the I/O space or the memory space, as needed. They can be fully decoded or partially decoded, depending on the application.

## PROBLEMS

1. A logician drives into a drive-in restaurant and says, "I want a hamburger or a hot dog and french fries." Unfortunately, the cook flunked out of sixth grade and does not know (or care) whether "and" has precedence over "or." As far as he is concerned, one interpretation is as good as the other. Which of the following cases are valid interpretations of the order? (Note that in English "or" means "exclusive or.")

   a. Just a hamburger.
   b. Just a hot dog.
   c. Just french fries.
   d. A hot dog and french fries.
   e. A hamburger and french fries.
   f. A hot dog and a hamburger.
   g. All three.
   h. Nothing—the logician goes hungry for being a wiseguy.

2. A missionary lost in Southern California stops at a fork in the road. He knows that two motorcycle gangs inhabit the area, one of which always tells the truth and one of which always lies. He wants to know which road leads to Disneyland. What question should he ask?

3. Use a truth table to show that $X = (X \text{ AND } Y) \text{ OR } (X \text{ AND NOT } Y)$.

4. There exist four Boolean functions of a single variable and 16 functions of two variables. How many functions of three variables are there? Of $n$ variables?

5. Show how the AND function can be constructed from two NAND gates.

6. Using the three-variable multiplexer chip of Fig. 3-12, implement a function whose output is the parity of the inputs, that is, the output is 1 if and only if an even number of inputs are 1.

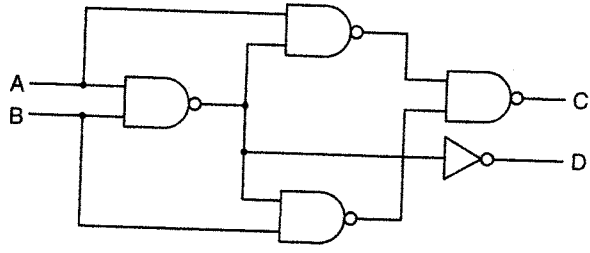
7. Put on your thinking cap. The three-variable multiplexer chip of Fig. 3-12 is actually capable of computing an arbitrary function of *four* Boolean variables. Describe how, and as an example, draw the logic diagram for the function that is 0 if the English word for the truth table row has an even number of letters, 1 if it has an odd number of letters (e.g., 0000 = zero = four letters $\rightarrow$ 0; 0111 = seven = five letters $\rightarrow$ 1; 1101 = thirteen = eight letters $\rightarrow$ 0). *Hint*: If we call the fourth input variable $D$, the eight input lines may be wired to $V_{cc}$, ground, $D$, or $\overline{D}$.

8. Draw the logic diagram of a 2-bit encoder, a circuit with four input lines, exactly one of which is high at any instant, and two output lines whose 2-bit binary value tells which input is high.

9. Draw the logic diagram of a 2-bit demultiplexer, a circuit whose single input line is steered to one of the four output lines depending on the state of the two control lines.

10. Redraw the PLA of Fig. 3-15 in enough detail to show how the majority logic function of Fig. 3-3 can be implemented. In particular, be sure to show which connections are present in both matrices.

11. What does this circuit do?




12. A common MSI chip is a 4-bit adder. Four of these chips can be hooked up to form a 16-bit adder. How many pins would you expect the 4-bit adder chip to have? Why?

13. An $n$-bit adder can be constructed by cascading $n$ full adders in series, with the carry into stage $i$, $C_i$, coming from the output of stage $i-1$. The carry into stage 0, $C_0$, is 0. If each stage takes $T$ nsec to produce its sum and carry, the carry into stage $i$ will not be valid until $iT$ nsec after the start of the addition. For large $n$ the time required for the carry to ripple through to the high-order stage may be unacceptably long. Design an adder that works faster. *Hint*: Each $C_i$ can be expressed in terms of the operand bits $A_{i-1}$ and $B_{i-1}$ as well as the carry $C_{i-1}$. Using this relation it is possible to express $C_i$ as a function of the inputs to stages 0 to $i-1$, so all the carries can be generated simultaneously.

14. If all the gates in Fig. 3-19 have a propagation delay of 1 nsec, and all other delays can be ignored, what is the earliest time a circuit using this design can be sure of having a valid output bit?

15. The ALU of Fig. 3-20 is capable of doing 8-bit 2's complement additions. Is it also capable of doing 2's complement subtractions? If so, explain how. If not, modify it to be able to do subtractions.

16. A 16-bit ALU is built up of 16 1-bit ALUs, each one having an add time of 10 nsec. If there is an additional 1 nsec delay for propagation from one ALU to the next, how long does it take for the result of a 16-bit add to appear?

17. Sometimes it is useful for an 8-bit ALU such as Fig. 3-20 to generate the constant $-1$ as output. Give two different ways this can be done. For each way, specify the values of the six control signals.

18. What is the quiescent state of the $S$ and $R$ inputs to an SR latch built of two NAND gates?

19. The circuit of Fig. 3-26 is a flip-flop that is triggered on the rising edge of the clock. Modify this circuit to produce a flip-flop that is triggered on the falling edge of the clock.

20. The $4 \times 3$ memory of Fig. 3-29 uses 22 AND gates and three OR gates. If the circuit were to be expanded to $256 \times 8$, how many of each would be needed?

21. To help meet the payments on your new personal computer, you have taken up consulting for fledgling SSI chip manufacturers. One of your clients is thinking about putting out a chip containing four D flip-flops, each containing both $Q$ and $\overline{Q}$, on request of a potentially important customer. The proposed design has all four clock signals ganged together, also on request. Neither preset nor clear is present. Your assignment is to give a professional evaluation of the design.

22. As more and more memory is squeezed onto a single chip, the number of pins needed to address it also increases. It is often inconvenient to have large numbers of address pins on a chip. Devise a way to address $2^n$ words of memory using fewer than $n$ pins.

23. A computer with a 32-bit wide data bus uses $1M \times 1$ dynamic RAM memory chips. What is the smallest memory (in bytes) that this computer can have?

24. Referring to the timing diagram of Fig. 3-38, suppose that you slowed the clock down to a period of 20 nsec instead of 10 nsec as shown but the timing constraints remained unchanged. How much time would the memory have to get the data onto the bus during $T_3$ after $\overline{\text{MREQ}}$ was asserted, in the worst case?

25. Again referring to Fig. 3-38, suppose that the clock remained at 100 MHz, but $T_{DS}$ was increased to 4 nsec. Could 10-nsec memory chips be used?

26. In Fig. 3-38(b), $T_{ML}$ is specified to be at least 3 nsec. Can you envision a chip in which it is negative? Specifically, could the CPU assert $\overline{\text{MREQ}}$ before the address was stable? Why or why not?

27. Assume that the block transfer of Fig. 3-42 were done on the bus of Fig. 3-38. How much more bandwidth is obtained by using a block transfer over individual transfers for long blocks? Now assume that the bus is 32 bits wide instead of 8 bits wide. Answer the question again.

**28.** Denote the transition times of the address lines of Fig. 3-39 as $T_{A1}$ and $T_{A2}$, and the transition times of $\overline{\text{MREQ}}$ as $T_{MREQ1}$ and $T_{MREQ2}$, and so on. Write down all the inequalities implied by the full handshake.

**29.** Most 32-bit buses permit 16-bit reads and writes. Is there any ambiguity about where to place the data? Discuss.

**30.** Many CPUs have a special bus cycle type for interrupt acknowledge. Why?

**31.** A 64-bit computer with a 200-MHz bus requires four cycles to read a 64-bit word. How much bus bandwidth does the CPU consume in the worst case?

**32.** A 32-bit CPU with address lines A2–A31 requires all memory references to be aligned. That is, words have to be addressed at multiples of 4 bytes, and half-words have to be addressed at even bytes. Bytes can be anywhere. How many legal combinations are there for memory reads, and how many pins are needed to express them? Give two answers and make a case for each one.

**33.** Why is it impossible for the Pentium 4 to work on a 32-bit PCI bus without losing any functionality? After all, other computers with a 64-bit data bus can do 32-bit, 16-bit, and even 8-bit wide transfers.

**34.** Suppose that a CPU has a level 1 cache and a level 2 cache, with access times of 1 nsec and 2 nsec, respectively. The main memory access time is 10 nsec. If 20% of the accesses are level 1 cache hits and 60% are level 2 cache hits, what is the average access time?

**35.** Is it likely that an 8051-based embedded system would include an 8255A chip?

**36.** Calculate the bus bandwidth needed to display a VGA ($640 \times 480$) true-color movie at 30 frames/sec. Assume that the data must pass over the bus twice, once from the CD-ROM to the memory and once from the memory to the screen.

**37.** Which Pentium 4 signal do you think drives the PCI bus FRAME# line?

**38.** Which of the signals of Fig. 3-56 is not strictly necessary for the bus protocol to work?

**39.** A PCI Express system has 5 Mbps links (gross capacity). How many signal wires are needed in each direction for 8x operation? What is the gross capacity each way? What is the net capacity each way?

**40.** A computer has instructions that each require two bus cycles, one to fetch the instruction and one to fetch the data. Each bus cycle takes 10 nsec and each instruction takes 20 nsec (i.e., the internal processing time is negligible). The computer also has a disk with 2048 512-byte sectors per track. Disk rotation time is 5 msec. To what percent of its normal speed is the computer reduced during a DMA transfer if each 32-bit DMA transfer takes one bus cycle?

**41.** The maximum payload of an isochronous data packet on the USB bus is 1023 bytes. Assuming that a device may send only one data packet per frame, what is the maximum bandwidth for a single isochronous device?

**42.** What would the effect be of adding a third input line to the NAND gate selecting the PIO of Fig. 3-62(b) if this new line were connected to A13?