Homework 3

ENEE 359a: Digital VLSI Design, Spring 2007
Assigned: Fri, Mar 9; Due: Tue, Mar 13

1. Transistor Sizing

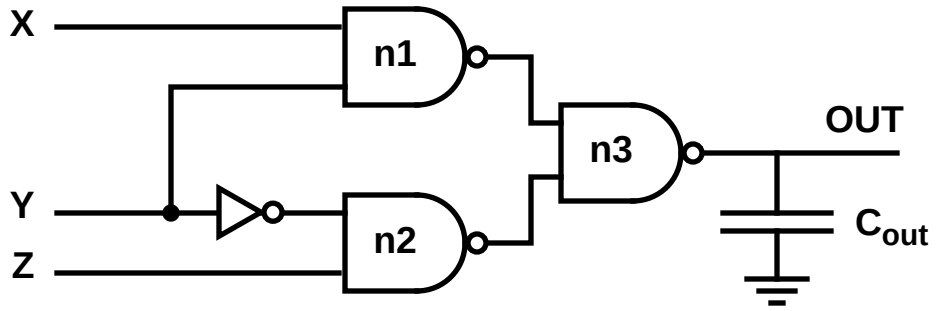
Consider a complex CMOS logic gate that implements the function Y = ~(ABC + DE + EFG).

A. Draw the transistor-level schematic of the gate.

B. Now optimize it: size all NMOS and PMOS transistors such that the worst-case rise and fall delays are equal to the fall delay of a minimum-sized CMOS inverter, assuming $R_p = 2.5\ R_n$.

2. Logical Effort

Consider the CMOS circuit shown below.



A. The critical path is through the inverter; ignoring the branching before this gate, use logical effort to size these gates to minimize the delay through the critical path. Assume $R_p = 2.5\ R_n$ and that all FETs in series have been scaled appropriately. Assume $C_{out} = 10\ C_{in}$ and that C_{in} applies to all inputs X, Y, and Z.

B. What is the minimum path delay through the inverter to OUT? You can assume that gamma=1 and that the p_i terms are all equal (leave symbolically as "p" in your answer).

C. How does this delay compare to the path delay from X to OUT through nand1 and nand3, now that nand3 has been optimized for the other path?