ENEE 359a
Digital VLSI Design

Some Parasitics
& How to Deal with Them

Prof. Bruce Jacob

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Credit where credit is due:
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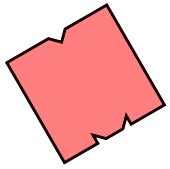
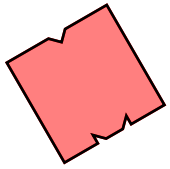


Overview

- ***Circuit Integrity*** **— Project-review presentation**
- **Capacitive Parasitics**
- **Resistive Parasitics**
- **Inductive Parasitics**



RF and Circuit Integrity in Digital Systems

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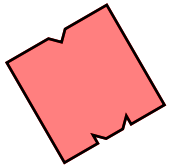
AFOSR-MURI Annual Review, October 2004



Overview

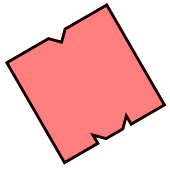
How Digital Circuits & Systems Are Built, and Some Ways in Which They Fail

- **Components of Digital Systems**
- **RF- and Temperature-Related Vulnerabilities**
  - ***Data*** *Inputs and Networks*
  - ***Clock*** *Inputs and Networks*
  - ***Power/Ground*** *Inputs and Networks*
- **Circuit Design: Our Device-Under-Test**

Recent Work

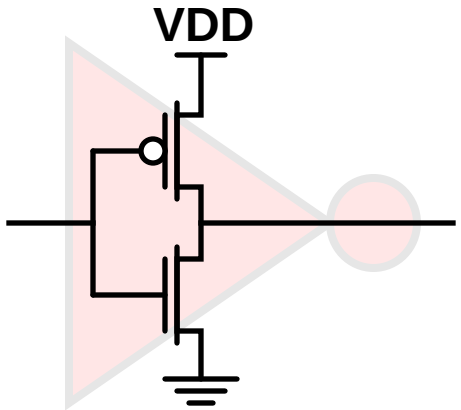
- **Comparison of Vulnerability: DUT's Clock/Data Inputs**
- **[DUT: test chip fabricated in AMI's 0.5µm process]**
- **Custom Chip Design & Fabrication for ESD Studies**

Future Work

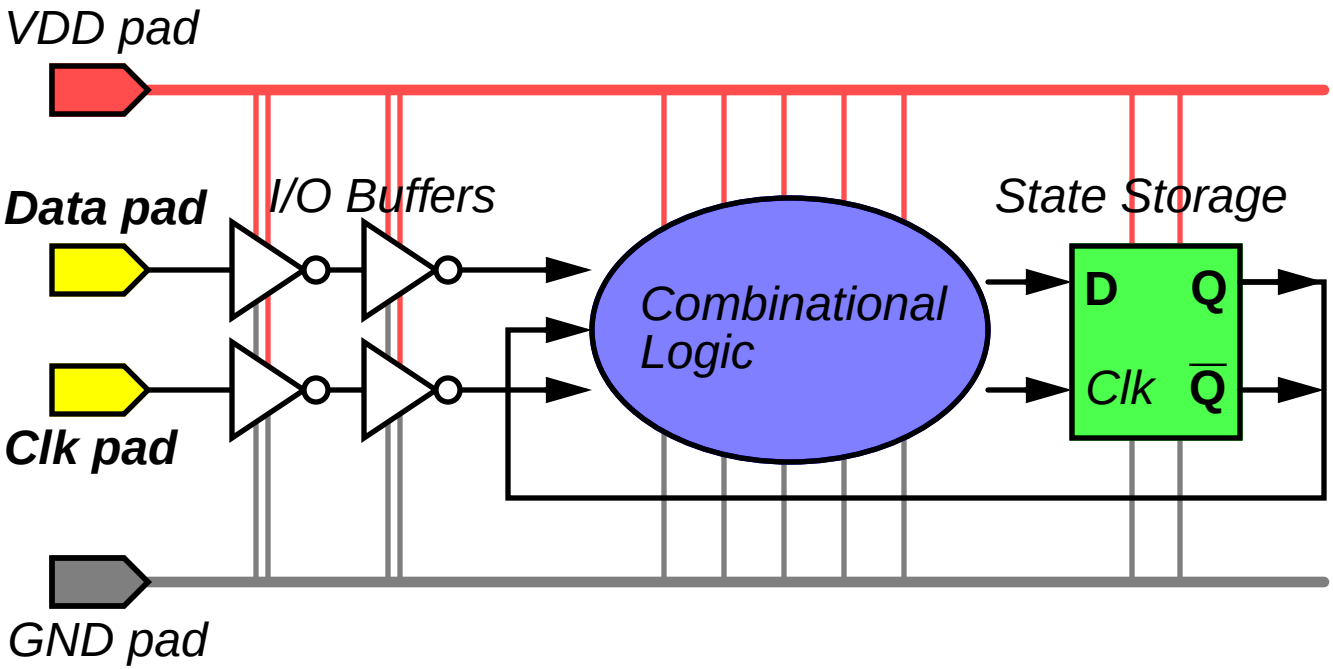


Digital Systems: A Primer

Simple Digital *Circuit:*

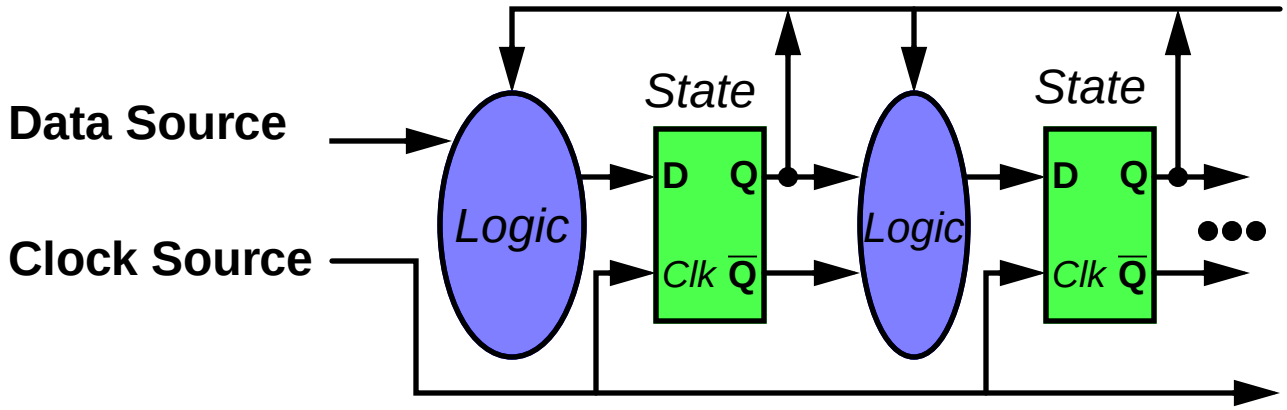


Simple Digital *System:*



Digital Systems: A Primer

Components of Digital Systems

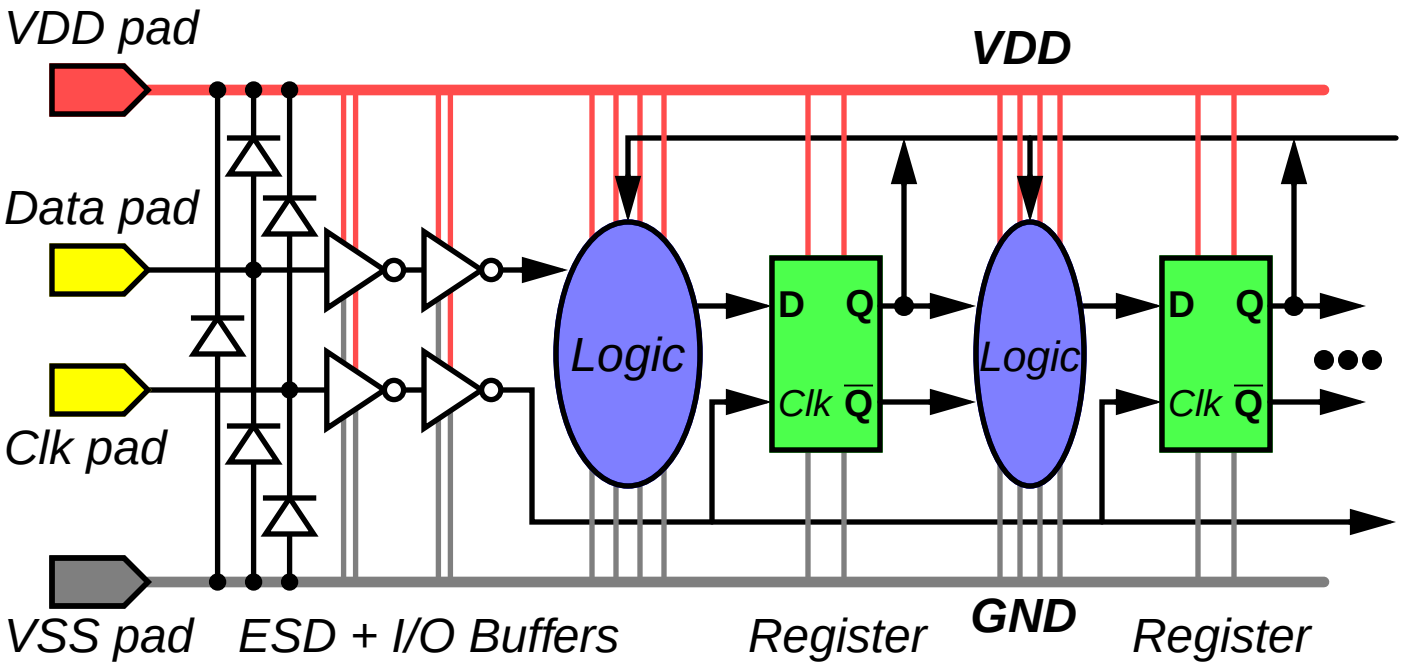


Most systems are *pipelined:*

- **Multiple logic blocks operating simultaneously**
- **Highly synchronous: lock-step operation**

Digital Systems: A Primer

Components of Digital Systems

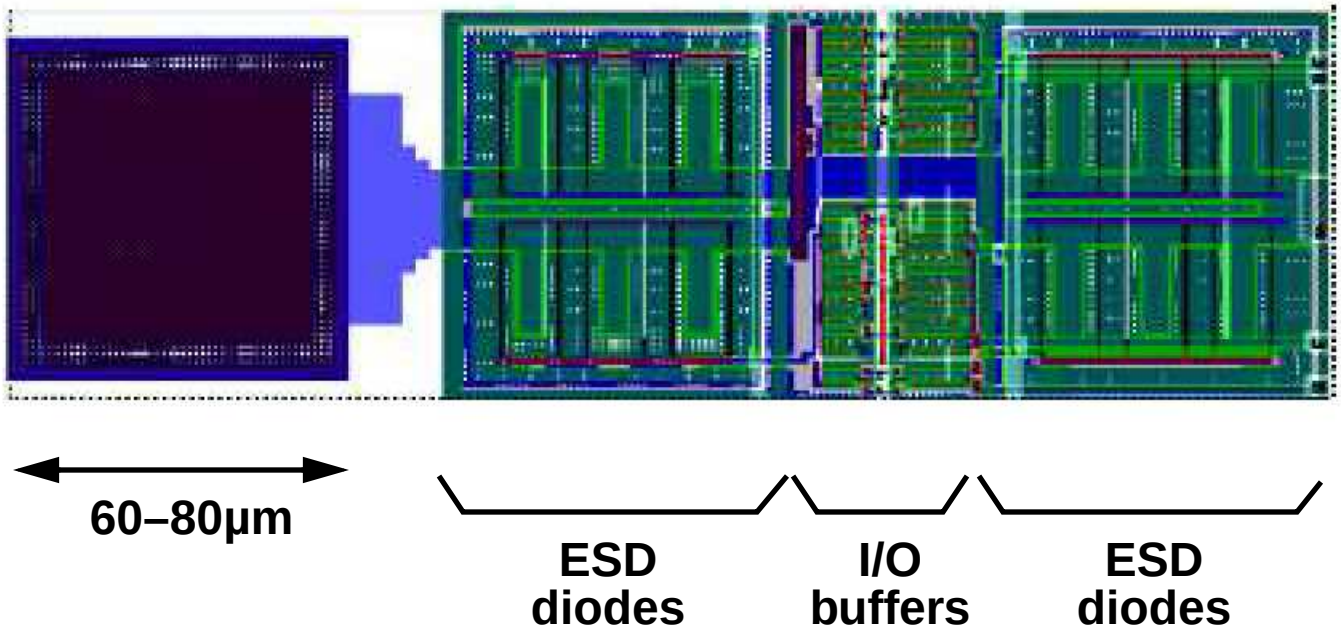


Groundplanes play significant role:

- **Provide references for input amplifiers**
- **Allow CMOS circuits to behave as signal repeaters (with high input impedance, low output impedance)**

Digital Systems: A Primer

Components of Digital Systems

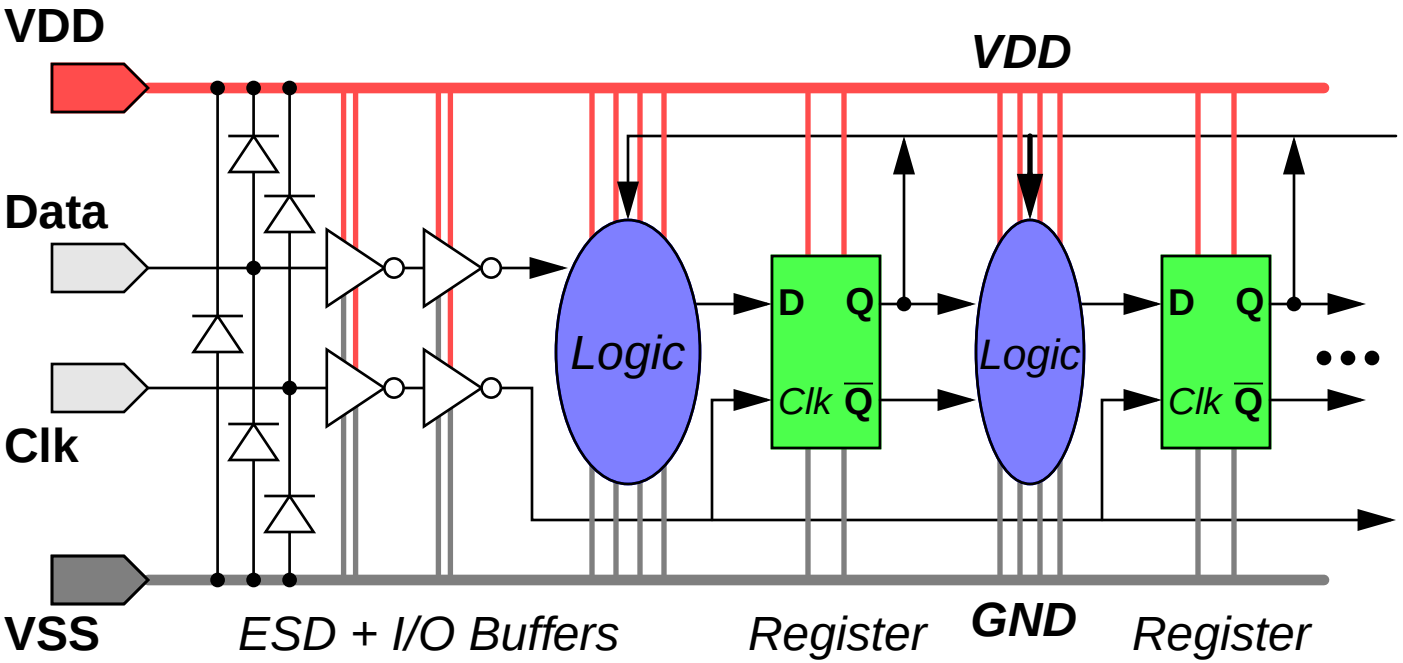


I/O Pads play significant role:

- **Enormous capacitances, require enormous gates to drive them (and the pins & off-chip traces)**
- **Big gates => big currents; fast clocks => small dt … VDD/VSS leads have inductance => Ldi/dt noise**

Digital Systems: A Primer

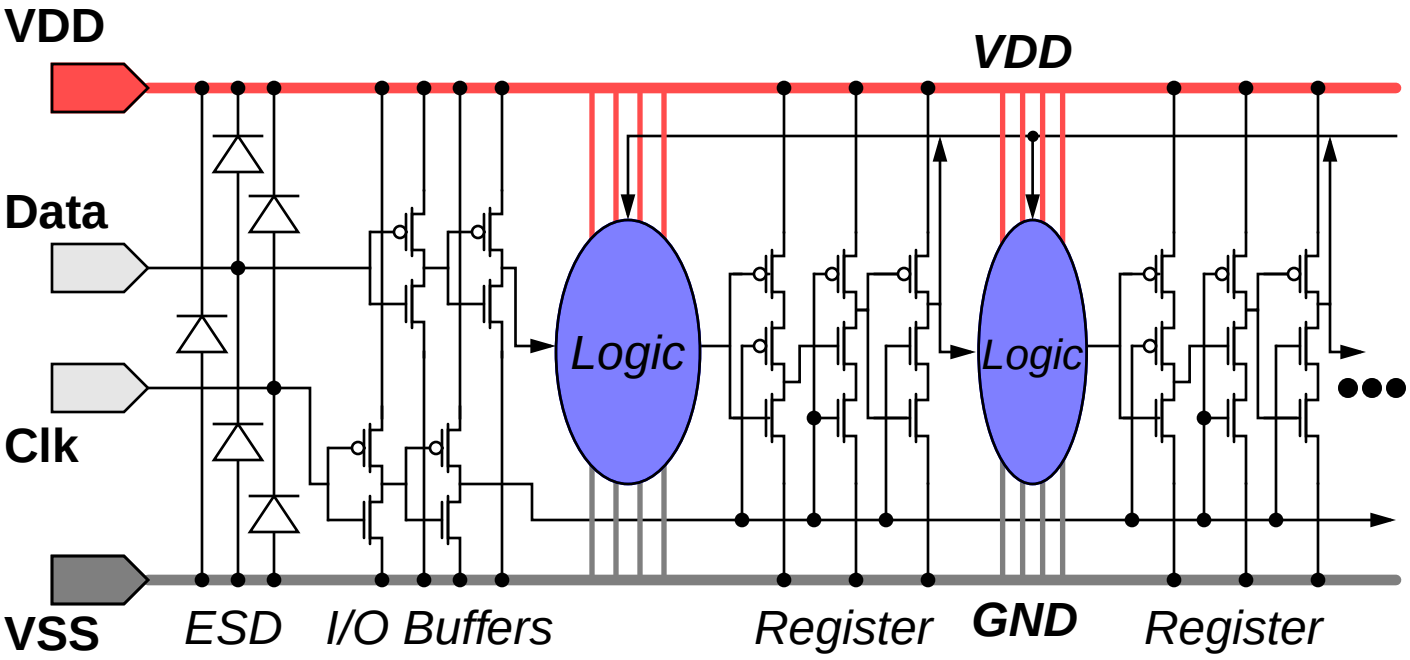
Components of Digital Systems



At the bottom are 'just' a bunch of MOSFETs

Digital Systems: A Primer

Components of Digital Systems

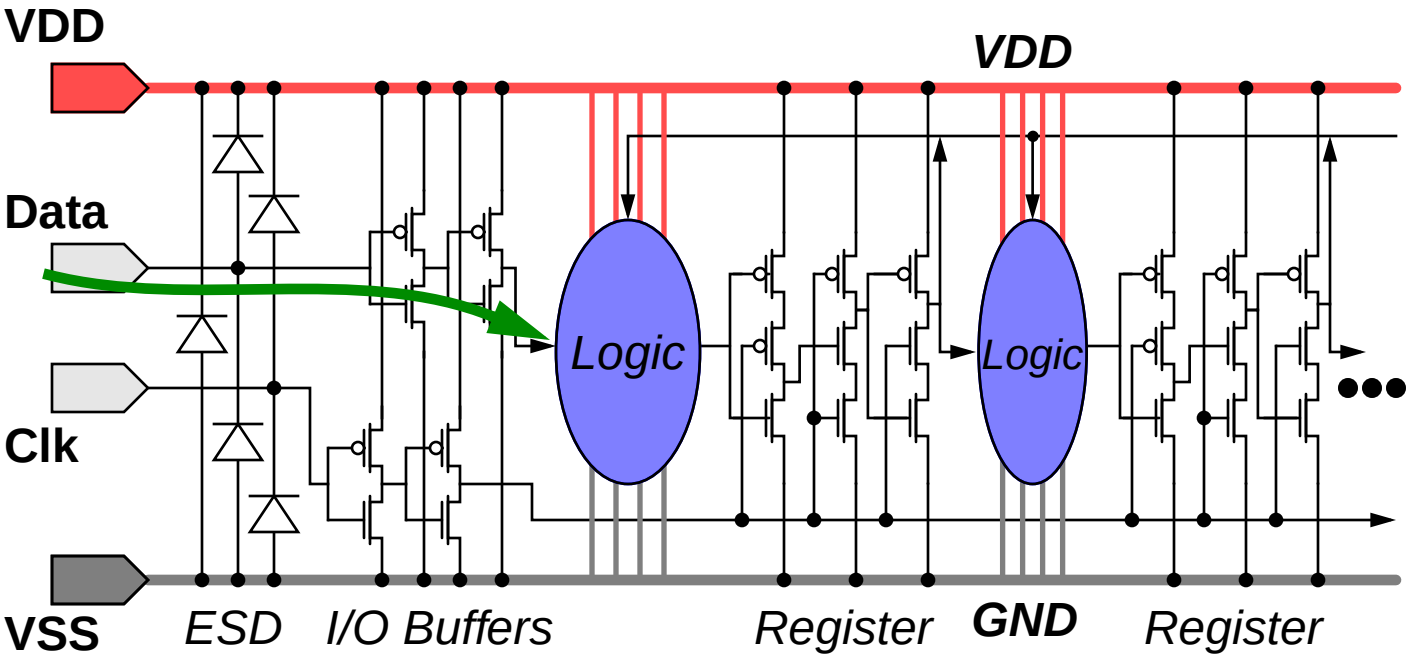


At the bottom are 'just' a bunch of MOSFETs

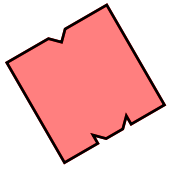
- Each register shown holds one bit
- Each I/O pad requires its own ESD, receivers, & drivers
- Logic blocks can be arbitrarily large/complex

Circuit Integrity: *Data*

How To Make This System Fail …

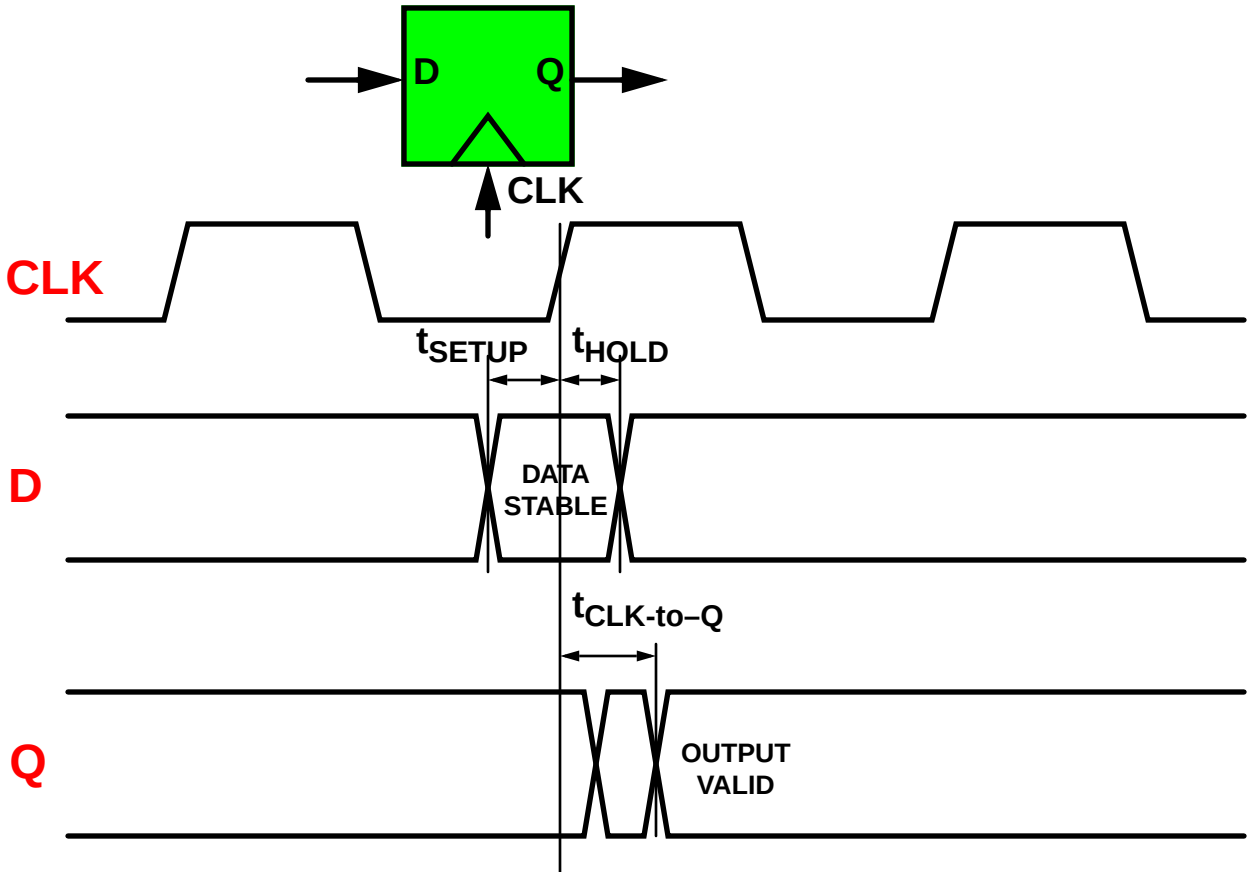


- **RF that makes it this far (past initial I/O buffers) has corrupted the system: only solution is to use higher level bus- or packet-encoding techniques**
- **Corrupted data can lead to incorrect results, software crash/reboot, transmission to remote nodes, etc.**

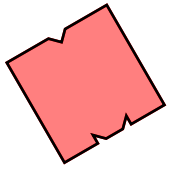


Sequential Circuits Primer

SET-UP and HOLD times

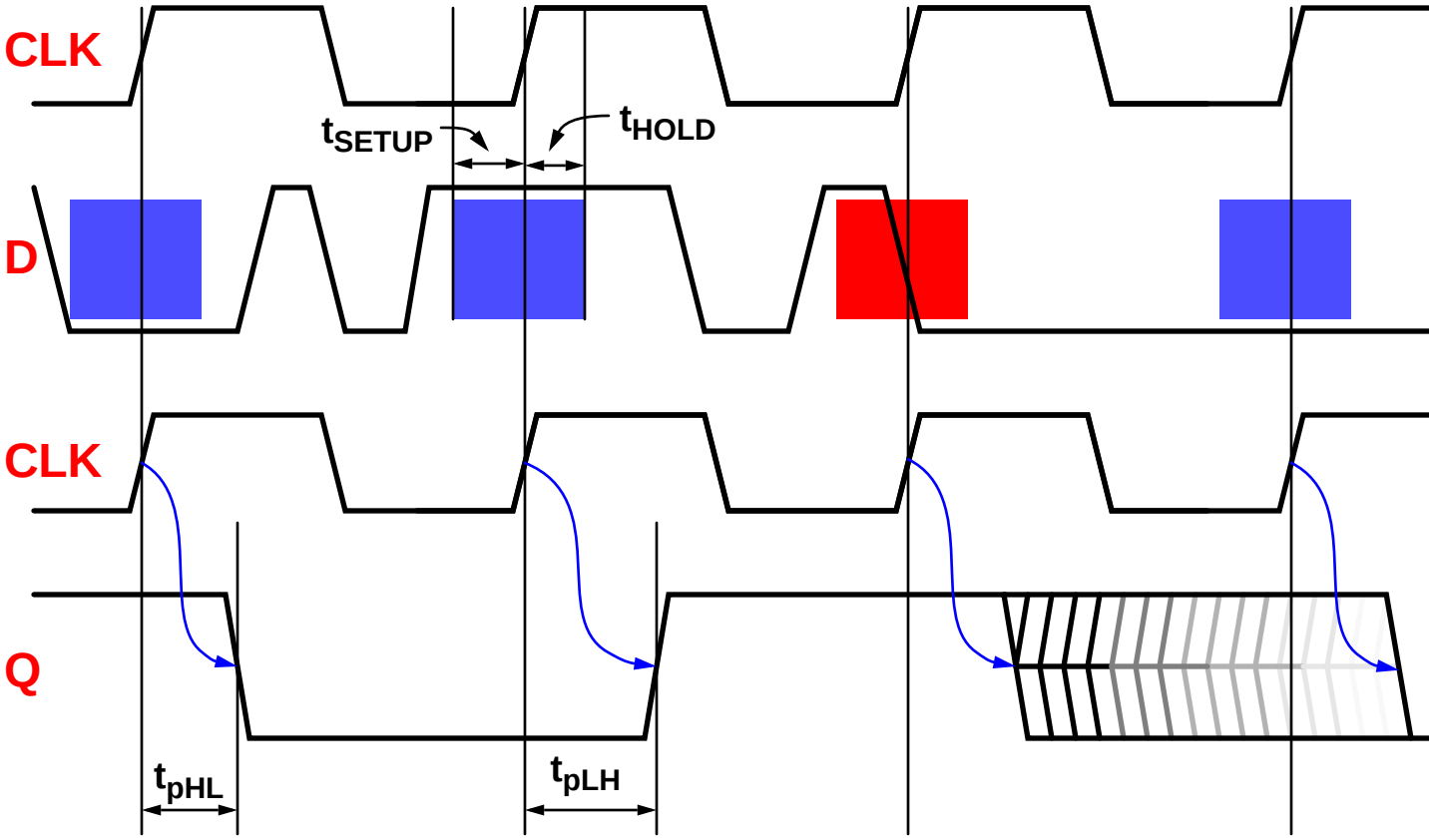


- **Storage elements (latches, registers) expect data and clock edges to be timed perfectly (e.g., within 20ps)**

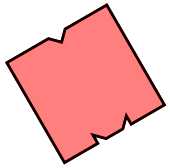


Sequential Circuits Primer

SET-UP and HOLD time, metastability

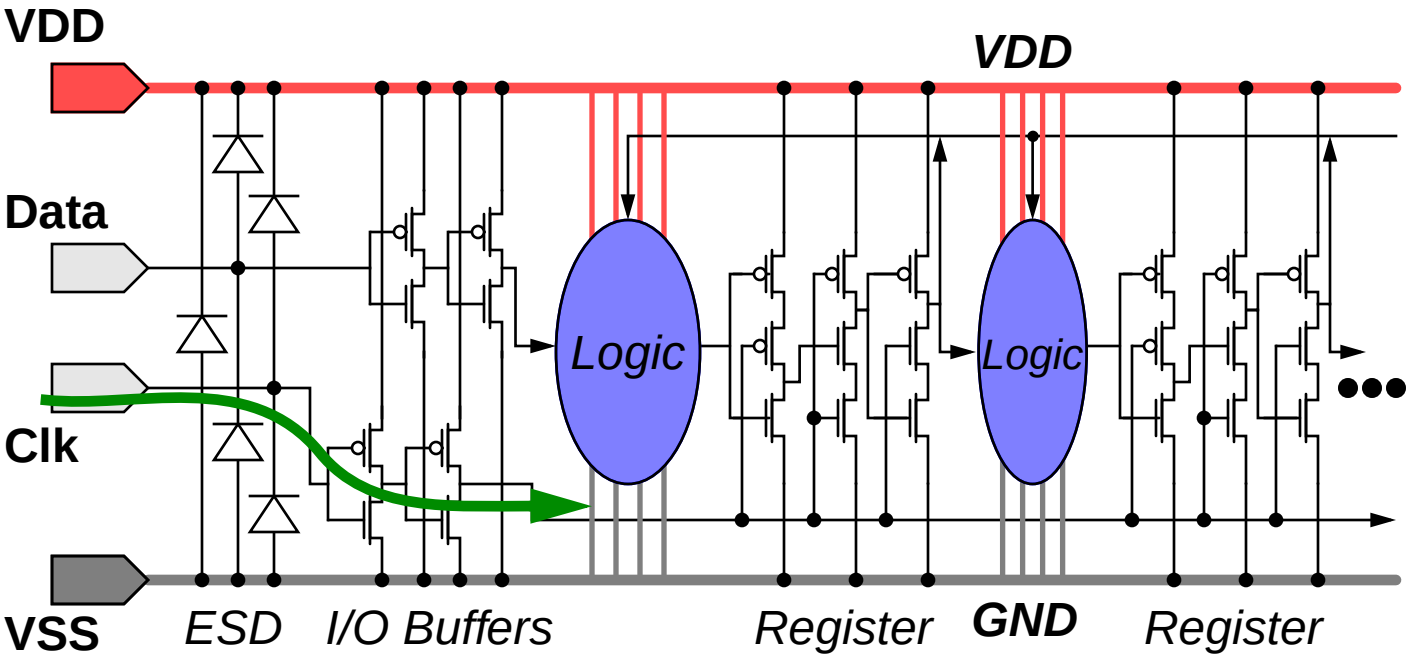


- **Data must not transition near clock edges**
- ***Corollary:* Perturbations on clock network (e.g., noise spikes, thermal-related delays) achieve same results**

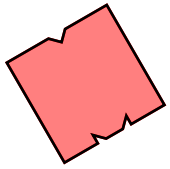


Circuit Integrity: *Clock*

How To Make This System Fail …

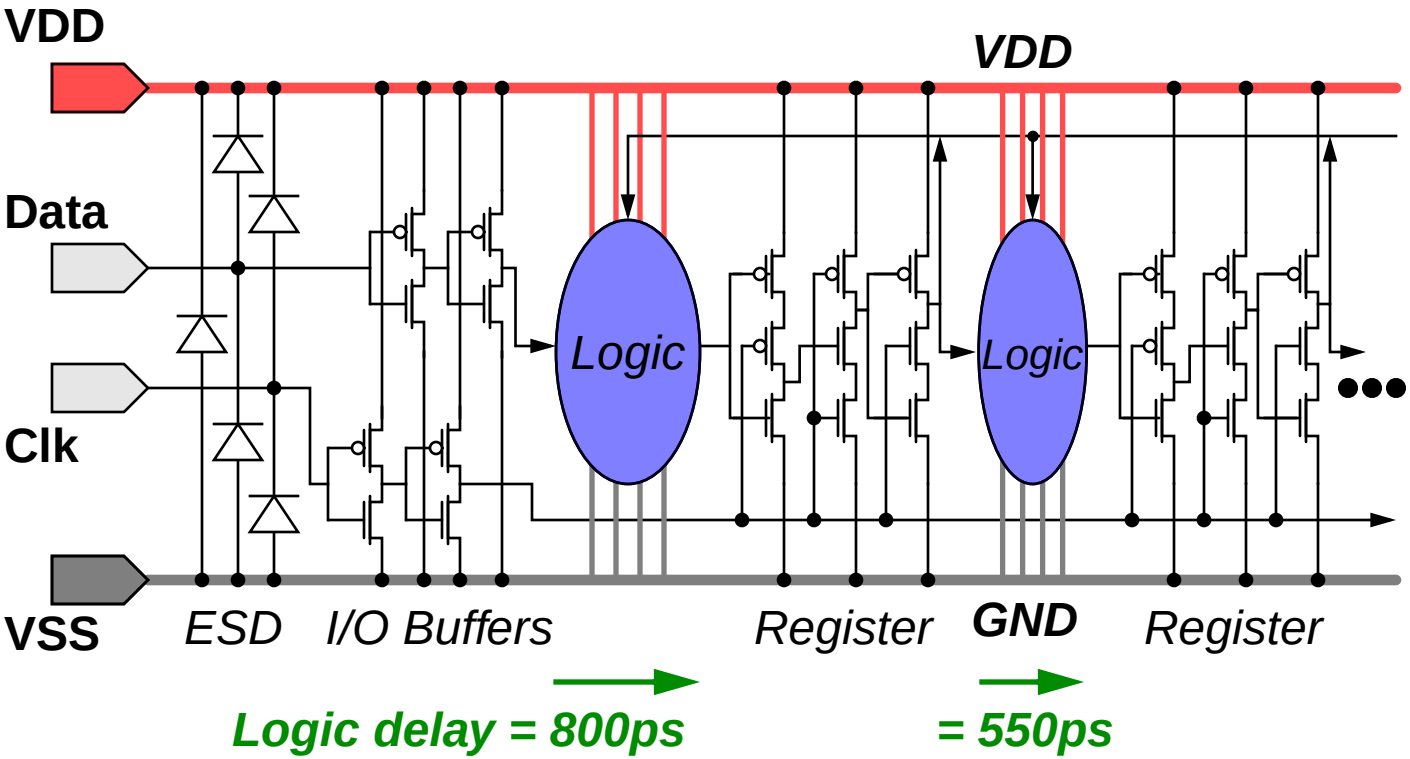


- **RF that makes it this far (past initial I/O buffers) has corrupted the system: packet-encoding techniques that might detect data corruption are inapplicable**
- **Unwanted clock edges likely result in metastability, lead to incorrect results, most likely system crash**



Circuit Integrity: *Clock*

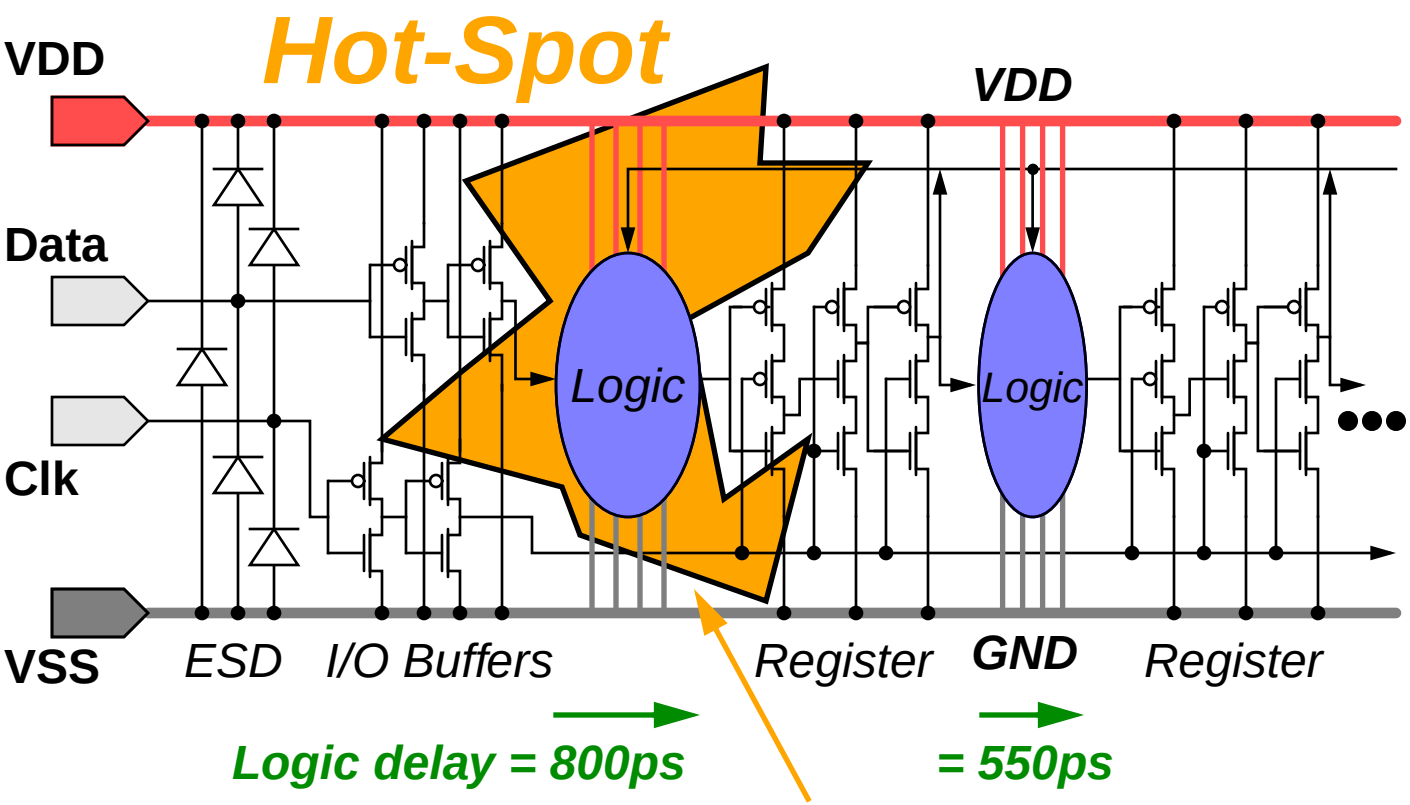
Maximum clock-frequency calculations



- **Critical path determines minimum clock period (in this example: 800ps + register overhead + skew/etc. =1000ps total, or 1GHz [as opposed to 750ps/1.33GHz])**

Circuit Integrity: *Clock*

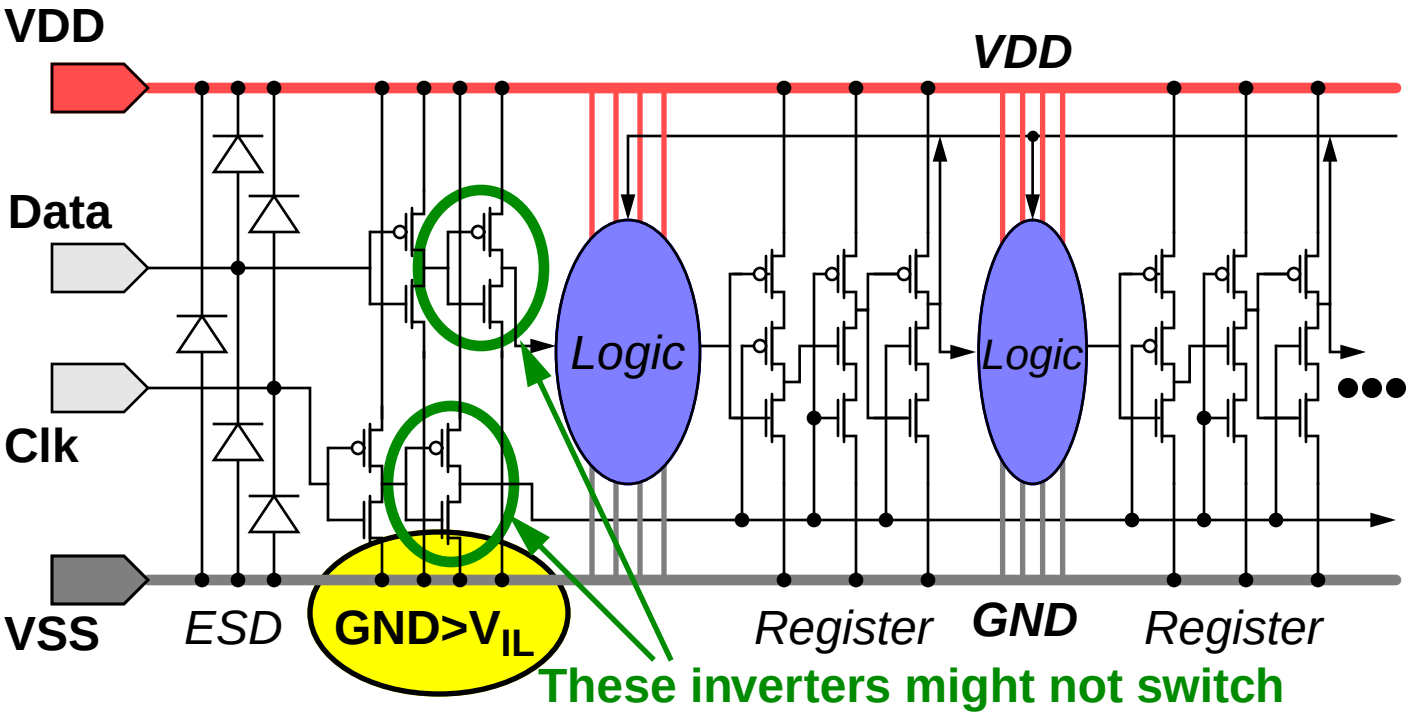
How To Make This System Fail …



- **Thermal gradients in synchronous systems disastrous (consider tight timing margins in GHz systems)**

Circuit Integrity: V_{DD} & V_{SS}

How To Make This System Fail …



- **Localized (or global) ripples on groundplanes can cause logic to misbehave, inputs to be misinterpreted (e.g. suppose Data/Clk = 1, V > V_{IL} on gate of 2nd INV)**
- **Causes same effects as data/clock corruption**

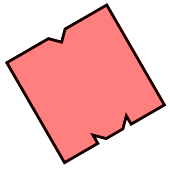
Circuit Integrity

DISTINGUISHING CHARACTERISTICS of the NETWORKS in DIGITAL SYSTEMS:

- **CLK: Only Edges Matter**
- **DATA: Both Timing and Levels Matter**
- **VDD/GND: Even Small Changes in Level (e.g., 5–10%) Matter**

CLK/DATA: Enter Via ESD Protection

VDD/GND: 1/2 ESD (shunts one to other)

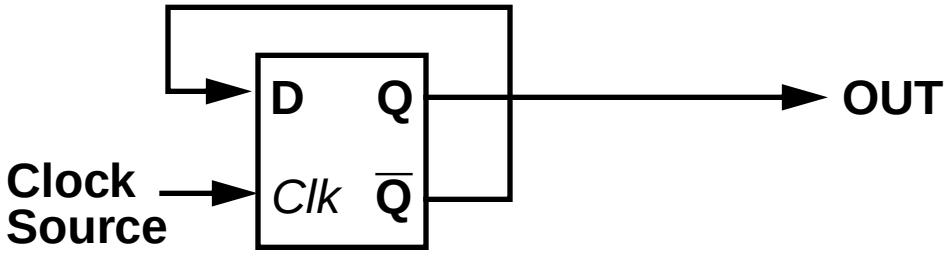


Our Research Question

Comparing CLK and DATA inputs, which is more important:

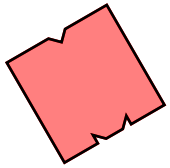
- **The distinguishing characteristics of the way those inputs will be used in the digital system or circuit?**
- **The levels and frequencies of injected RF?**

Our Device Under Test (counter):

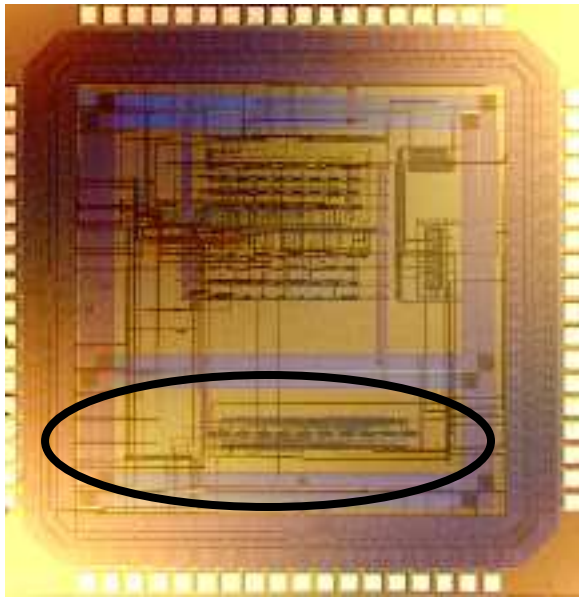


Just about simplest possible digital system

[*Last Year's Results:* evaluated vulnerability of CLK input]



Our Device Under Test



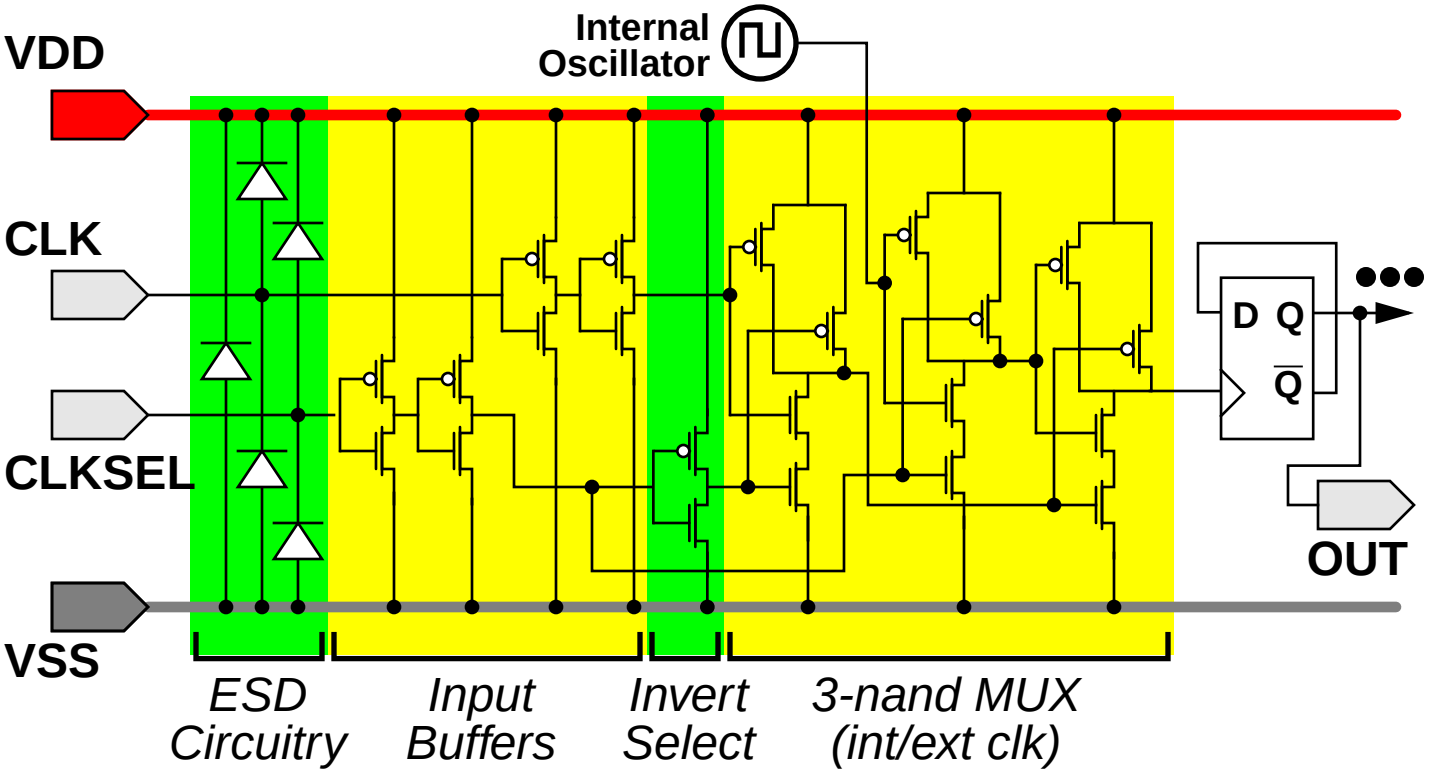
8-bit Ripple Counter, Chip Built via MOSIS

Full-Custom Design (except for pad frame)

Fabricated in AMI's 0.5µm Technology

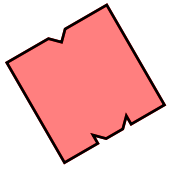
3.3V power supply

Our Device Under Test

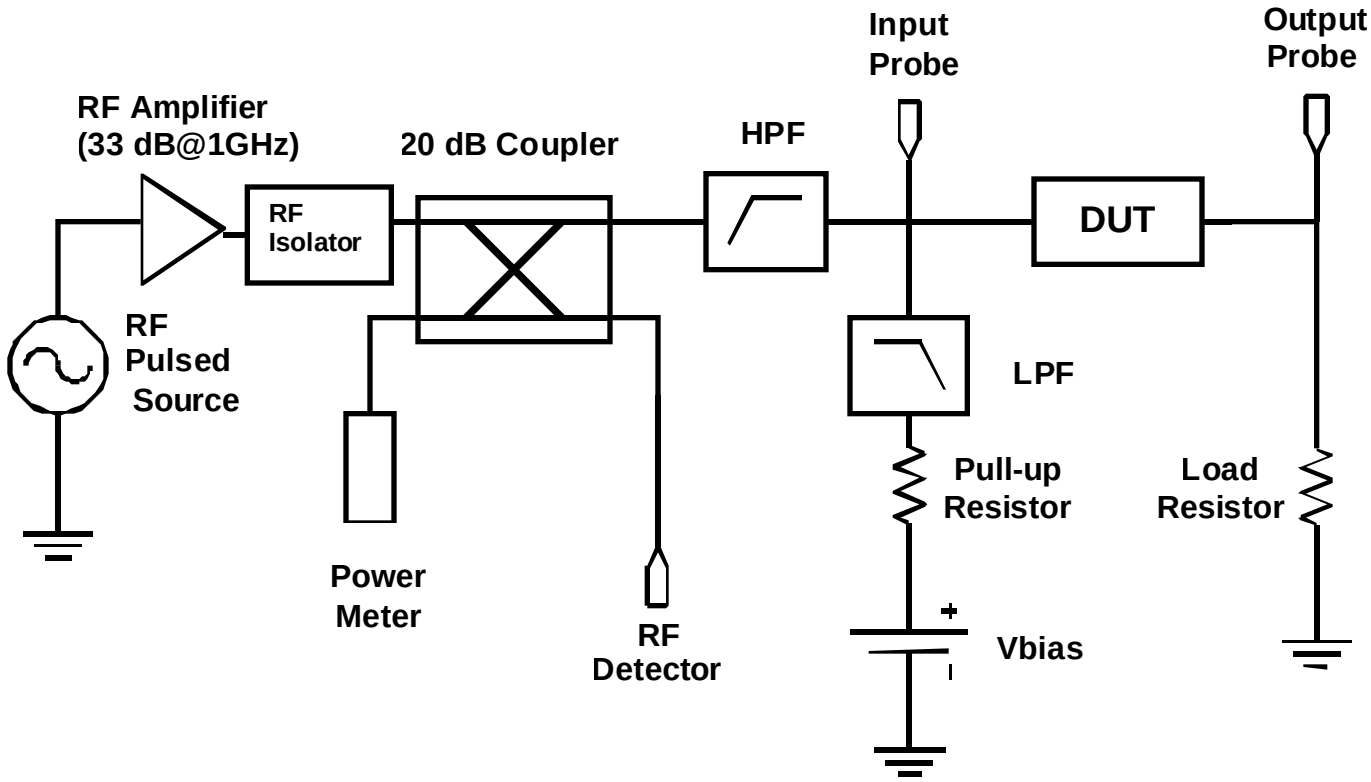


Points of Interest:

- **Digital system built from complementary gate designs (high input impedance, low output impedance).**
- **CLK only driving MUX, one DFF (*see previous slide*).**
- **=> CLK and CLKSEL see virtually identical loads.**



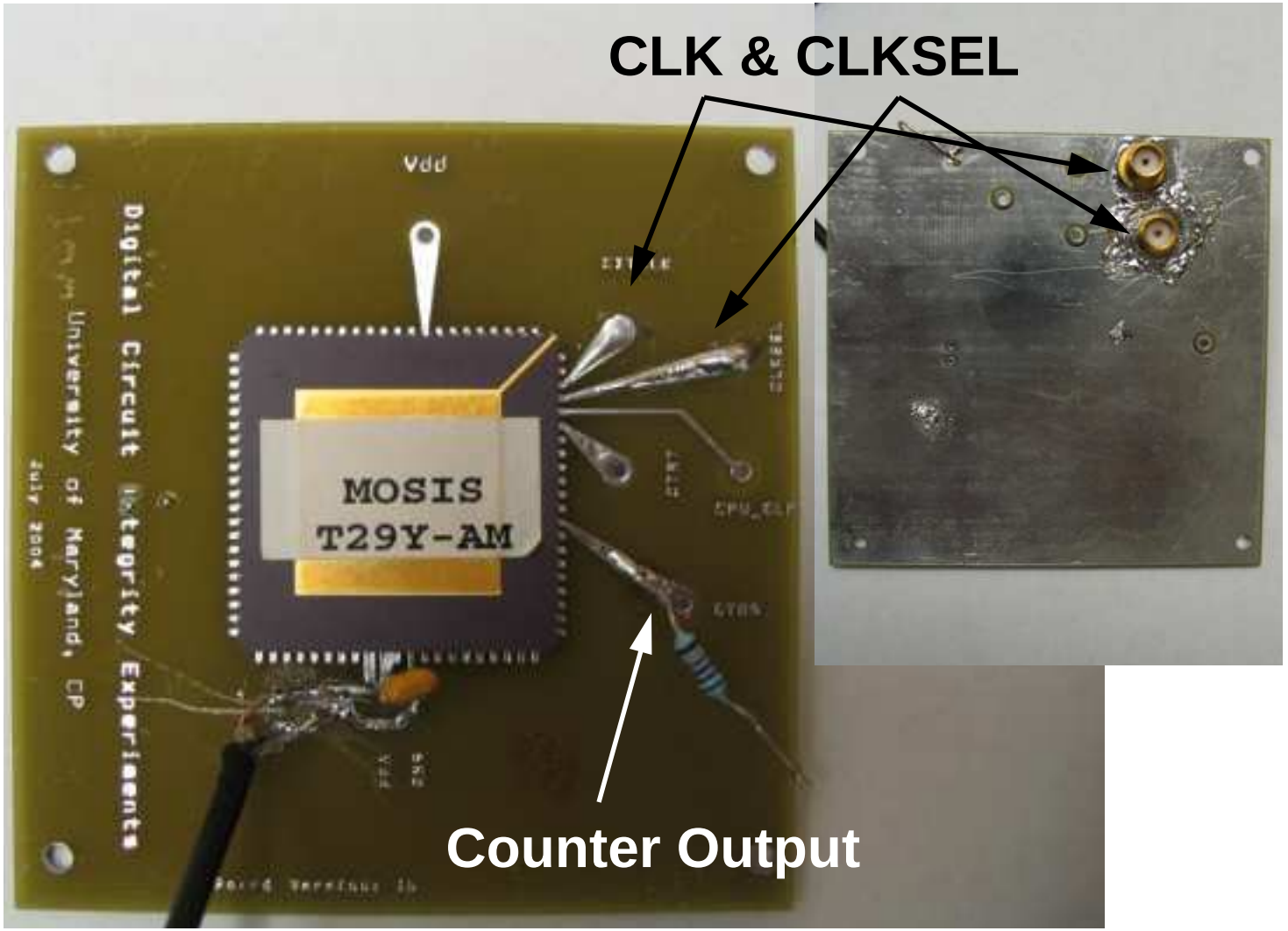
Experimental RF Set-Up



Power Amp 33dB at 1GHz

Freq 800MHz – 4.2Ghz with 1.2W max power

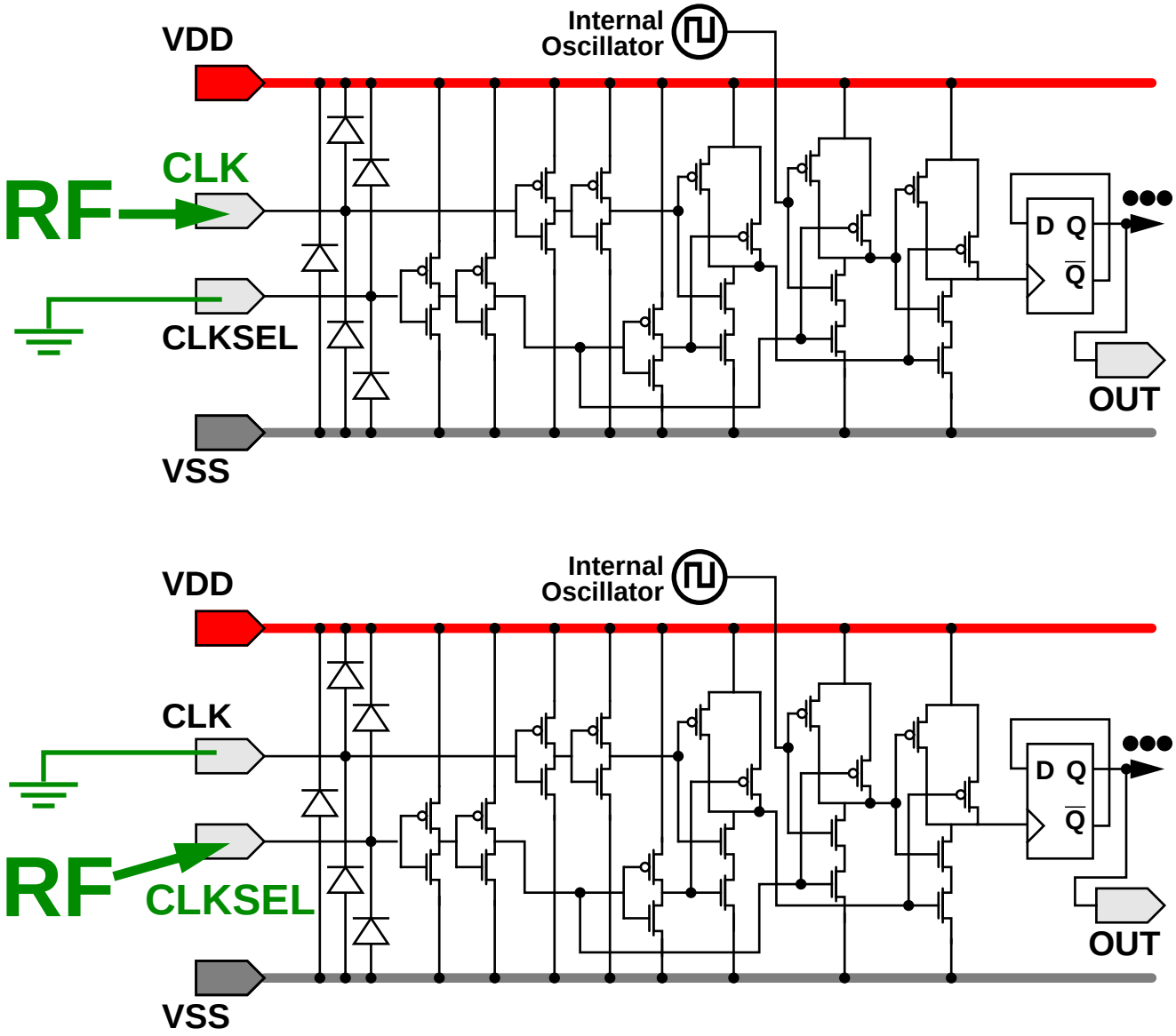
Test Board

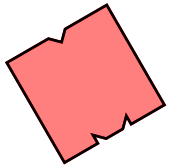

CLK & CLKSEL
Vdd
MOSIS
T29Y-AM
Digital Circuit Integrity Experiments
University of Maryland, CP
July 2004
Counter Output

Bruce Jacob

University of
Maryland
ECE Dept.

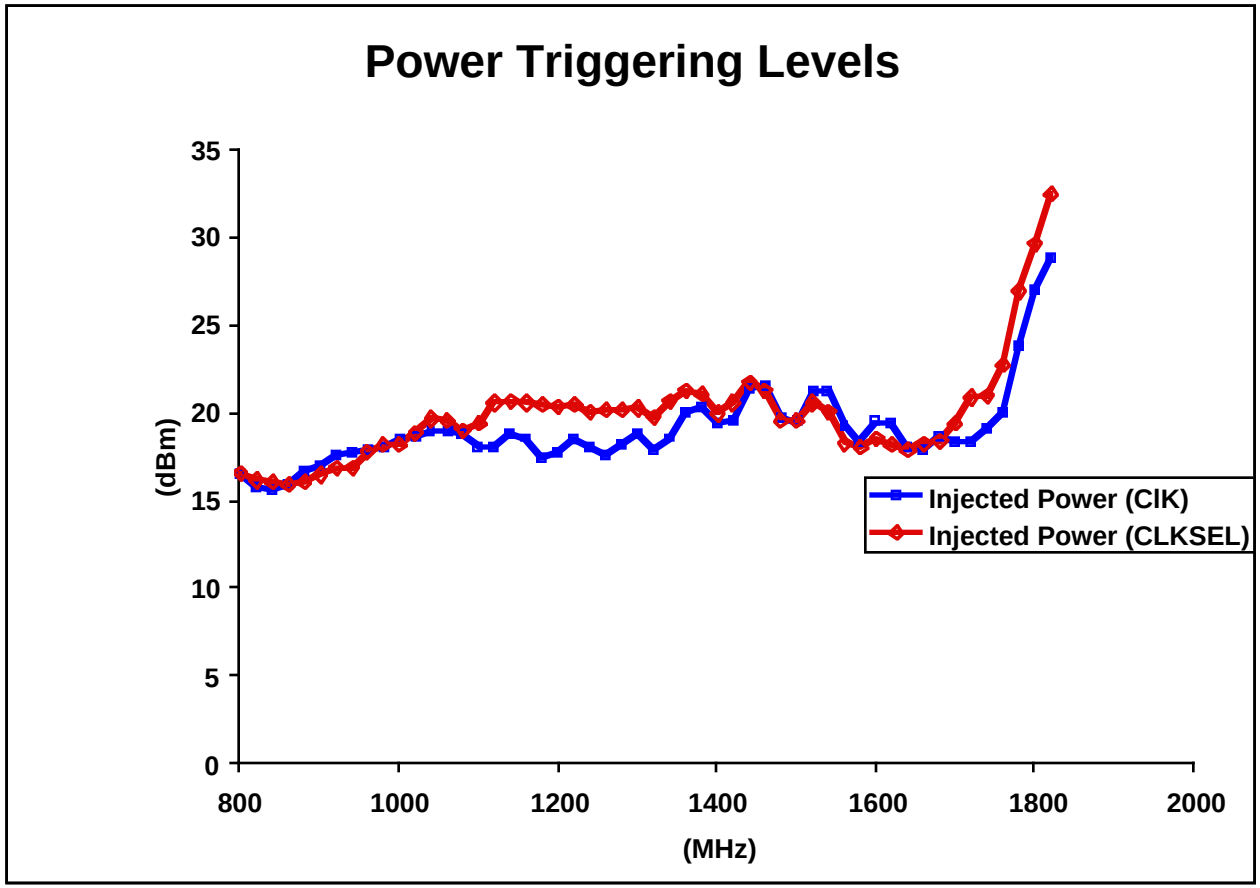
Test Scenarios





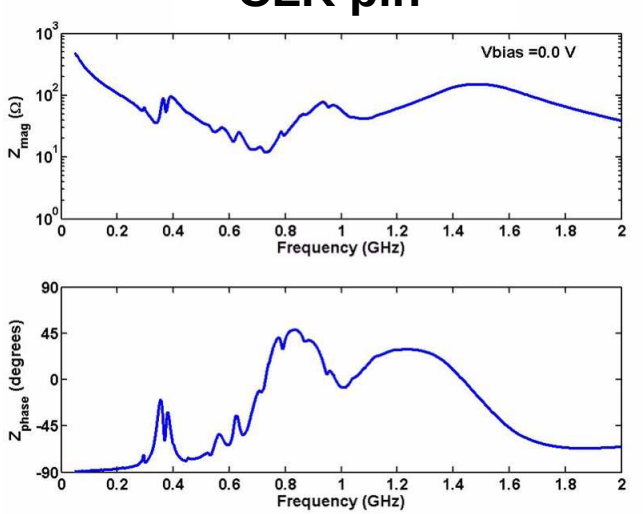
CLK vs. CLKSEL Inputs

Power-v-Freq. required to cause incorrect behavior (state change in digital logic)

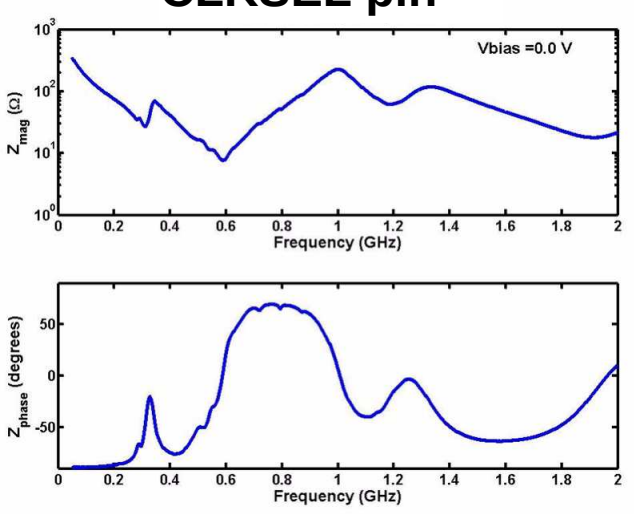


Input Impedance

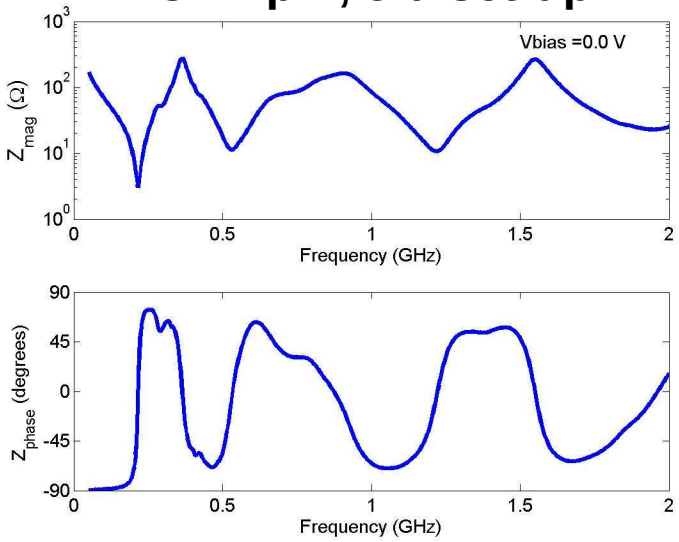
CLK pin

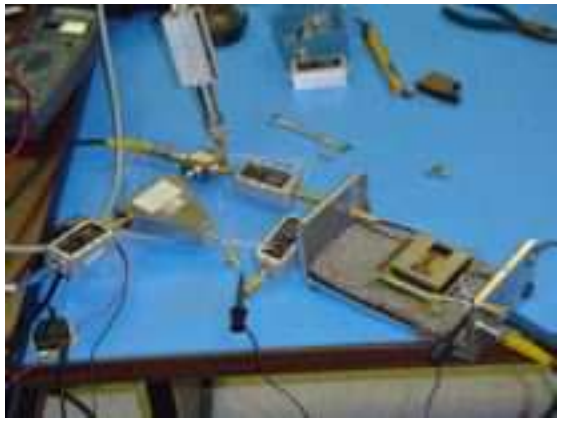


CLKSEL pin



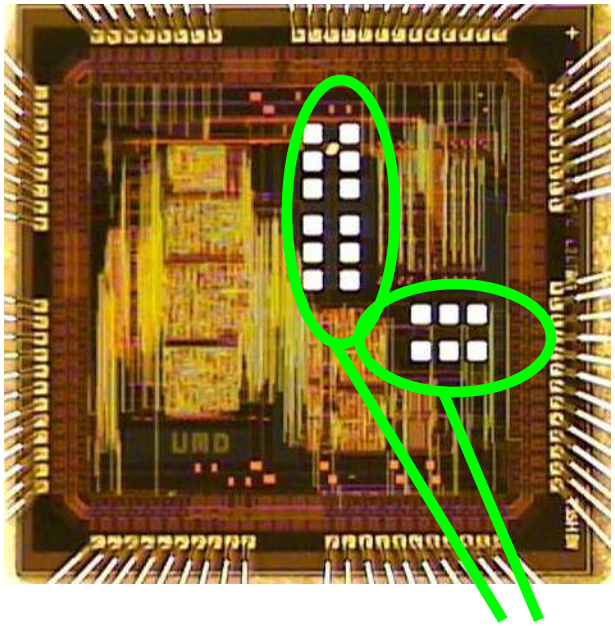
CLK pin, old set-up



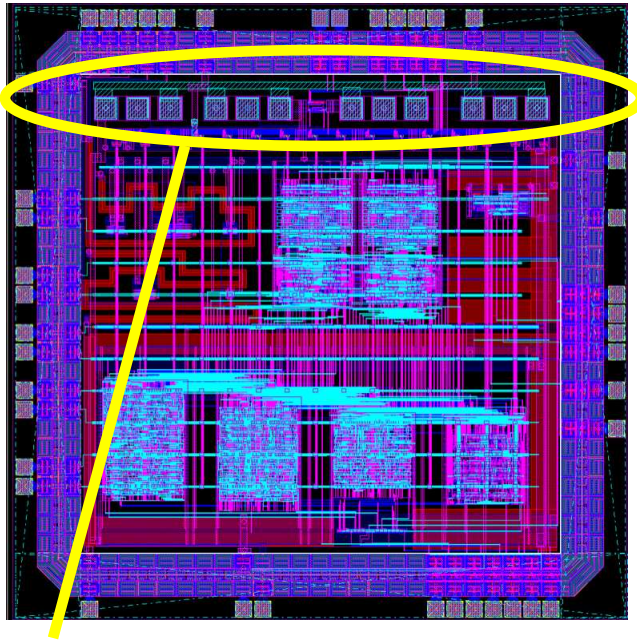


Recent Work: ESD

ESD Test Chip I (die photo)
for Rodgers & Firestone



ESD Test Chip II (layout)
for Rodgers & Firestone

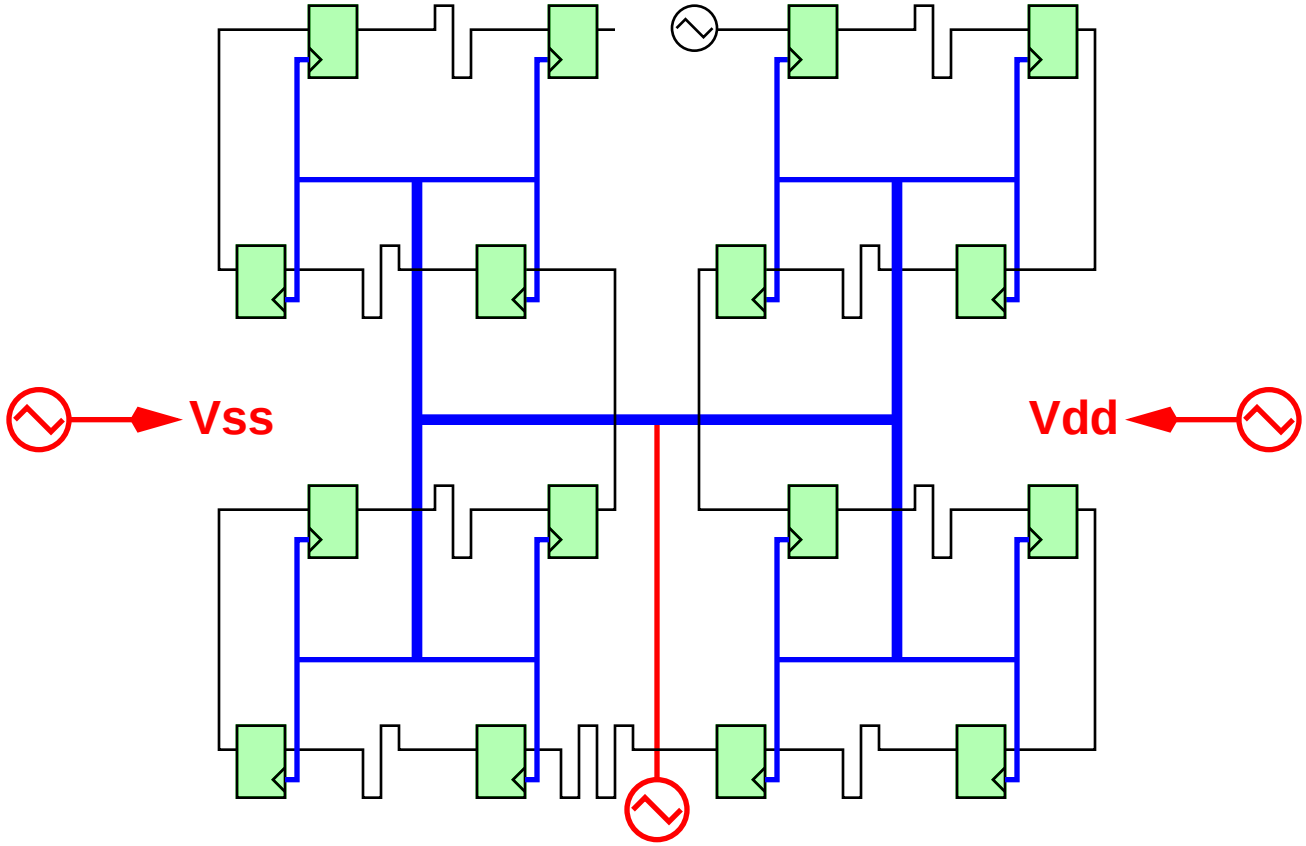


Custom-designed on-chip pads to accommodate input probes

Designed & fabricated two chips (one on right just back from fab) … allow probing at various points between PAD and internals

Future Work

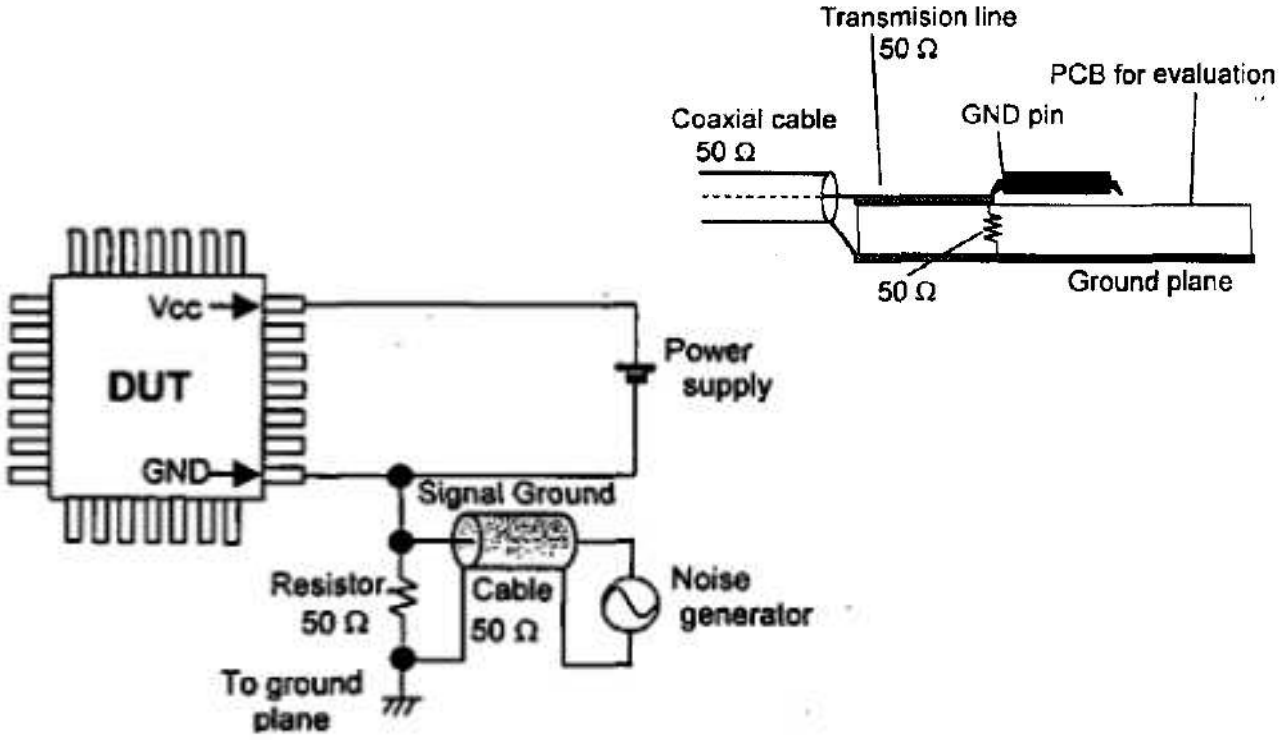
New Test Structures (e.g., to emulate larger designs, differentiate between CLK & DATA)



Future Work

Using same board, test the power rail

Design new board that differentiates GND input pin from IC's ground plane, to test the ground pin's susceptibility



Acknowledgments, etc.

GRAD STUDENTS:

Vincent Chan, Cagdas Dirik,
Samuel Rodriguez, Hongxia Wang

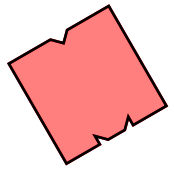
INVALUABLE AID:

Todd Firestone and John Rodgers

FOR MORE INFO:

http://www.ece.umd.edu/~blj/integrity

blj@umd.edu



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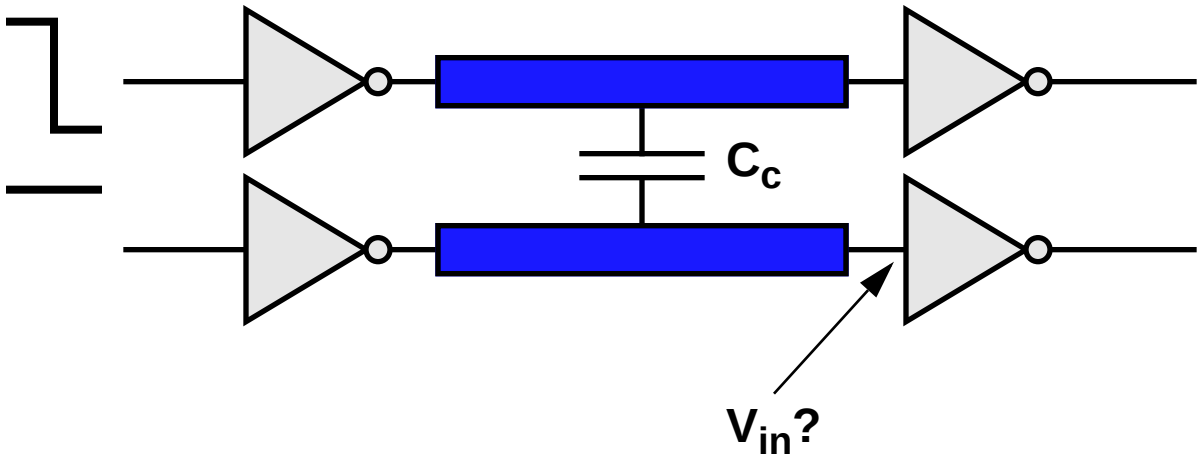
Capacitive Parasitics

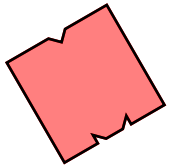
CROSS TALK

Largely capacitive at current switching speeds … inductive coupling is major concern in I/O of mixed signal circuits (e.g. RF).

Translation: *pay attention to the cut-off frequency*.



In general, $V_{in} \neq 0$

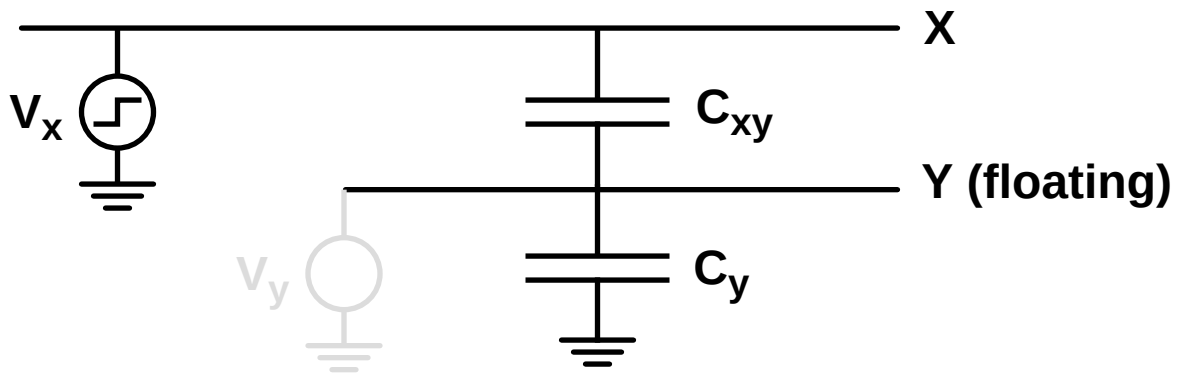


Capacitive Coupling

Influenced by *impedance* of coupled line:

- **Wire Y is driven: ΔV_y is transient**
- **Wire Y is floating: ΔV_y is *persistent***

Floating:



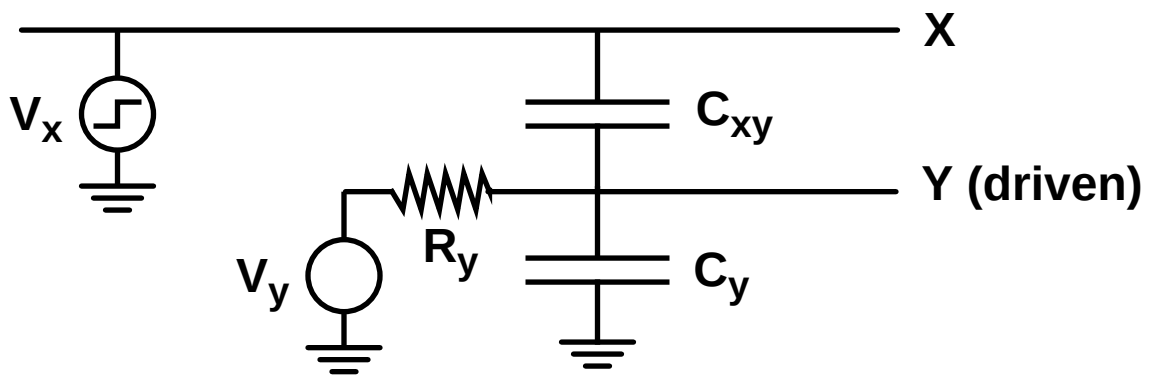
$$\Delta V_y = \Delta V_x \bullet \frac{C_{xy}}{C_y + C_{xy}}$$

Capacitive Coupling

Influenced by *impedance* of coupled line:

- **Wire Y is driven: ΔV_y is transient**
- **Wire Y is floating: ΔV_y is *persistent***

Driven:

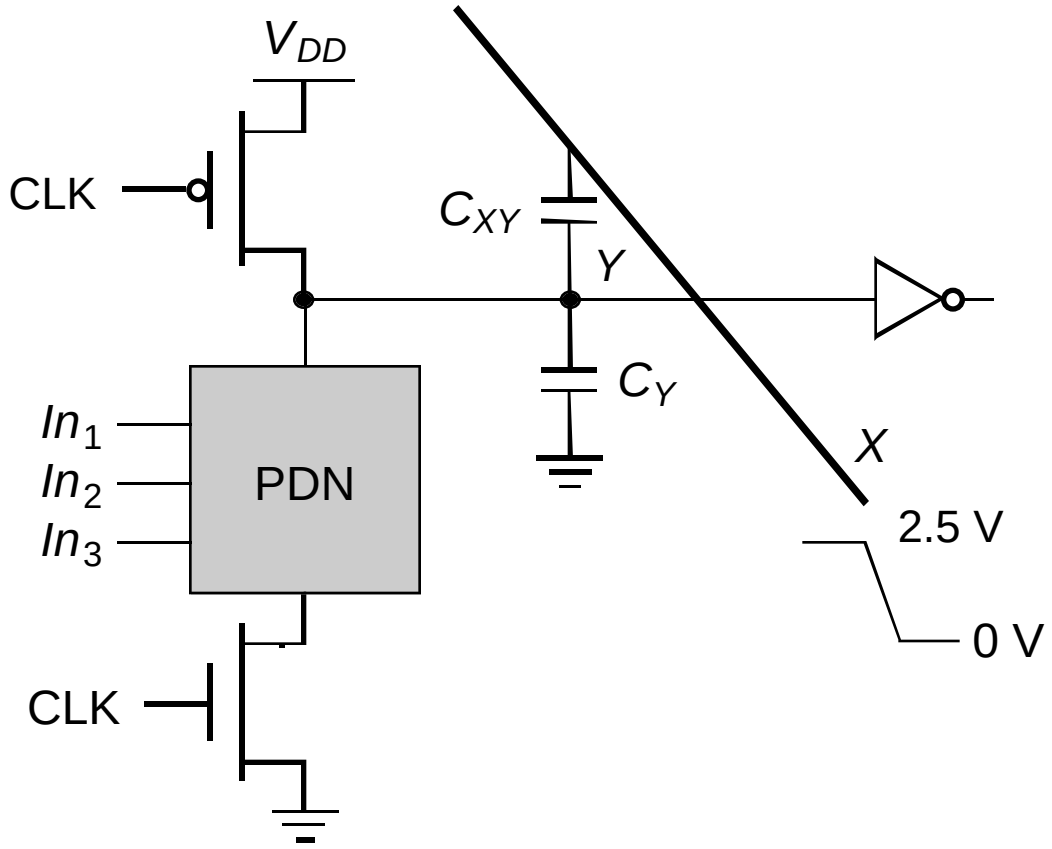


$$\Delta V_y = \Delta V_x \bullet \frac{Z_y \bullet C_{xy}}{t_{rise}}$$

Floating-Coupling Example

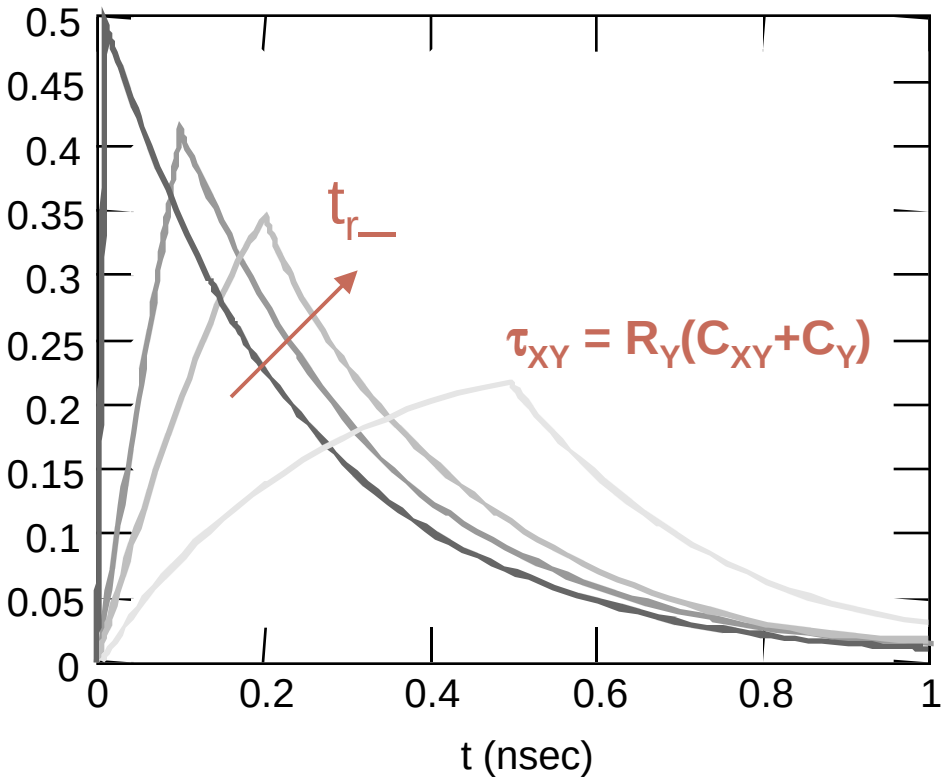
X is (logically unrelated) wire crossing over circuit in the metal-1 layer. Because this is a dynamic circuit, the output is floating when PDN=>false.

Example assumes capacitance to poly wire Y (gate for inverter); node Y is precharged during PRE stage to 2.5V, wire X undergoes 2.5 -> 0V.



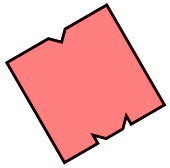
3 x 1 μm overlap: 0.19 V disturbance

Driven-Coupling Example



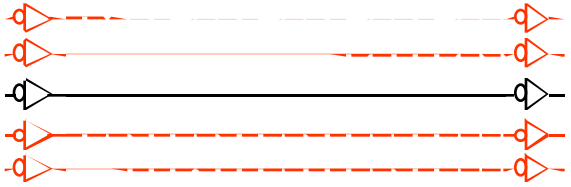
Transient decays with time constant

$$\tau_{xy} = R_y(C_{xy} + C_y)$$



Crosstalk & Technology

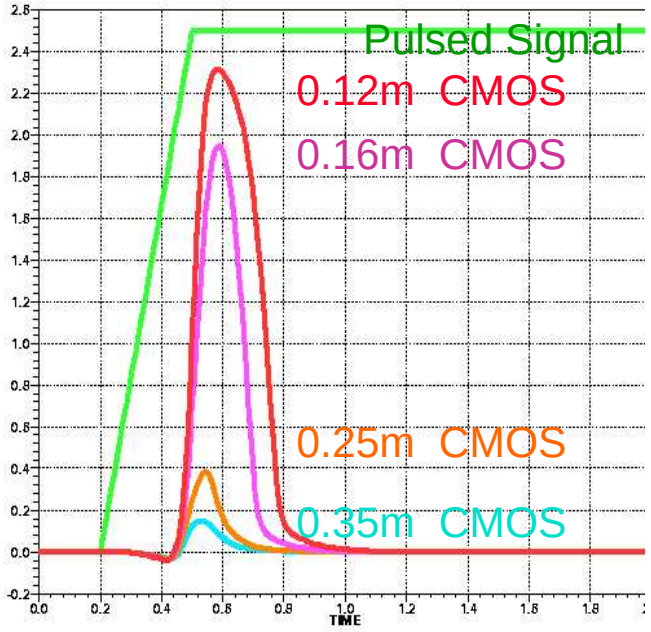
Crosstalk vs. Technology



Black line quiet

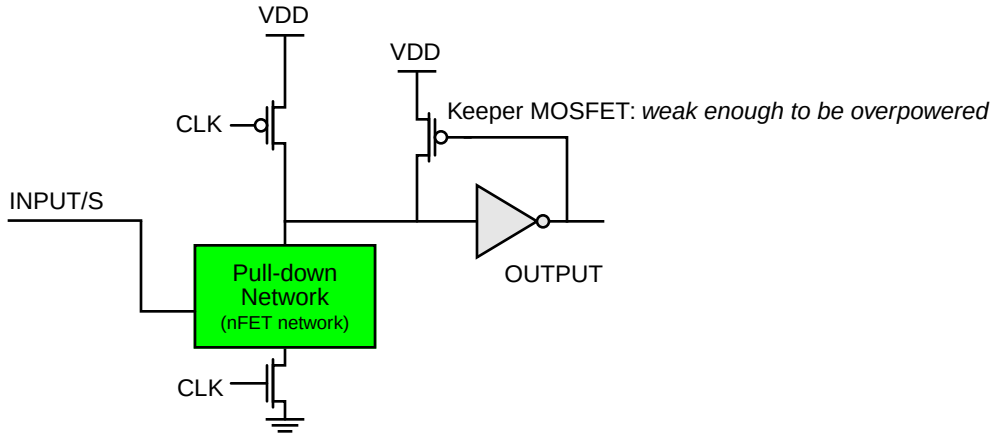
Red lines pulsed

Glitches strength vs technology

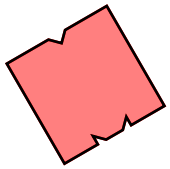


Some Solutions to Capacitive Crosstalk

- **Proportional noise source: Increasing Vdd will not help**
- **Avoid floating nodes: use "keeper" circuits, e.g.:**

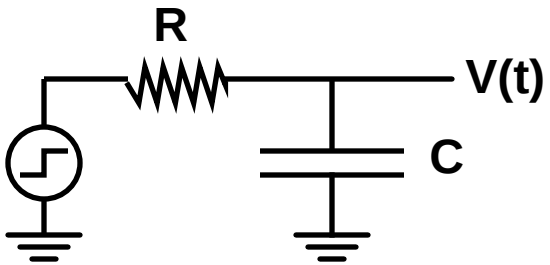


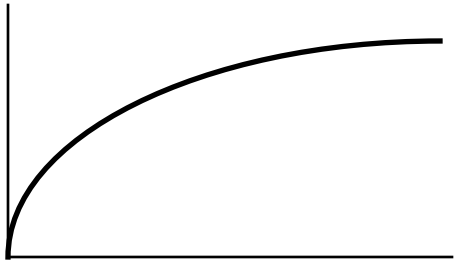
- **Keep sensitive nodes from full-swing signals**
- **Make rise/fall time large (but it can increase power)**
- **Use differential signaling: turns cross-talk into "common-mode" noise source**
- **Don't have long parallel wires**
- **Wires on adjacent metal levels: *perpendicular***
- **Shield wires by inserting VDD/GND wires between (works in same plane as well as in vertical dimension)**



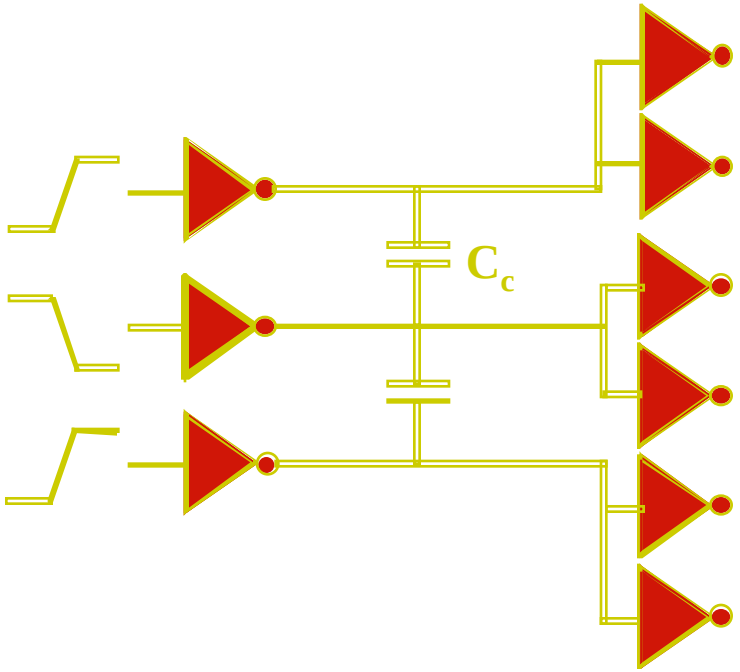
Capacitance & Wire Delays

Recall rise time:





What if is C is not a constant?



Miller Effect

Both terminals of capacitor are switched in opposite directions

(0 -> Vdd, Vdd -> 0)

Effective voltage is doubled and additional charge is needed

(from Q=CV)

Bottom Line:

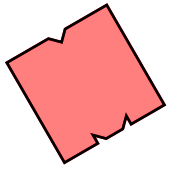
RC time constant doubles.

Capacitance & Wire Delays

- **r is ratio between capacitance to neighbor and to GND:**

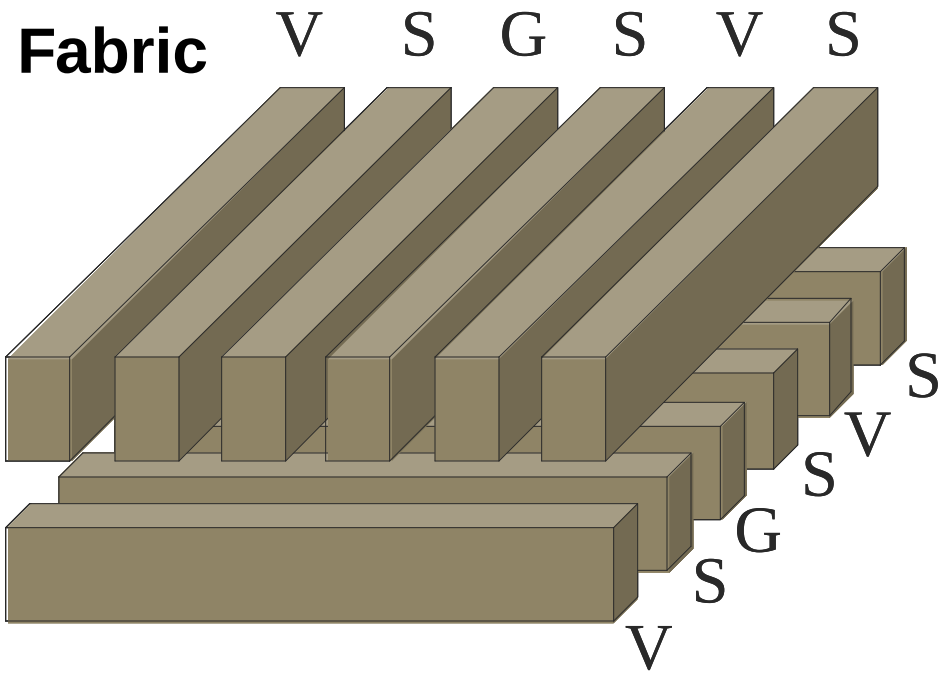
bit $k-1$	bit k	bit $k+1$	Delay factor g
↑	↑	↑	1
↑	↑	—	$1+r$
↑	↑	↓	$1+2r$
—	↑	—	$1+2r$
—	↑	↓	$1+3r$
↓	↑	↓	$1+4r$

- **Wire delay may vary over 500% between worst & best case, due solely to activity on wires**



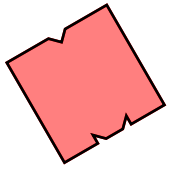
Solutions to Wire-Delay Prob.

Dense Wire Fabric



Trade-off:

- **Cross-coupling capacitance 40x lower, 2% delay variation**
- **Increase in area and overall capacitance**



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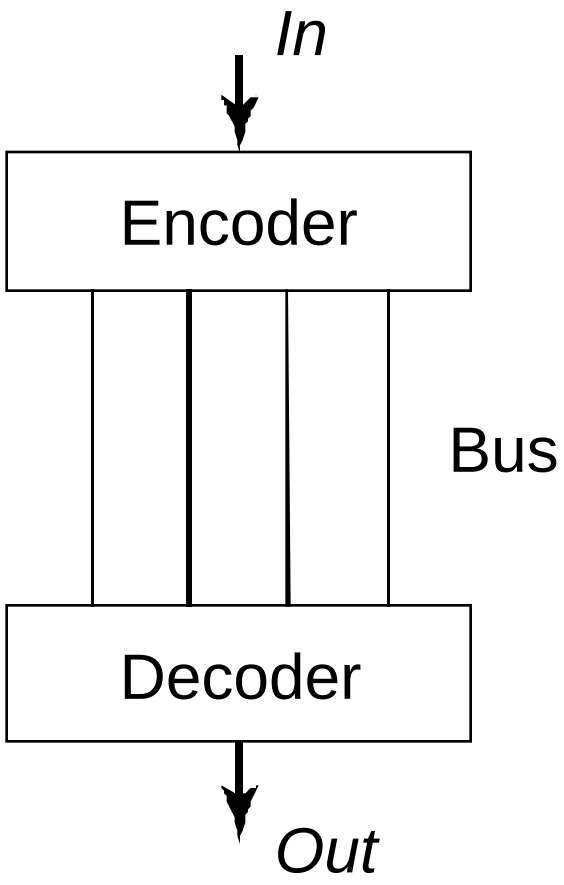
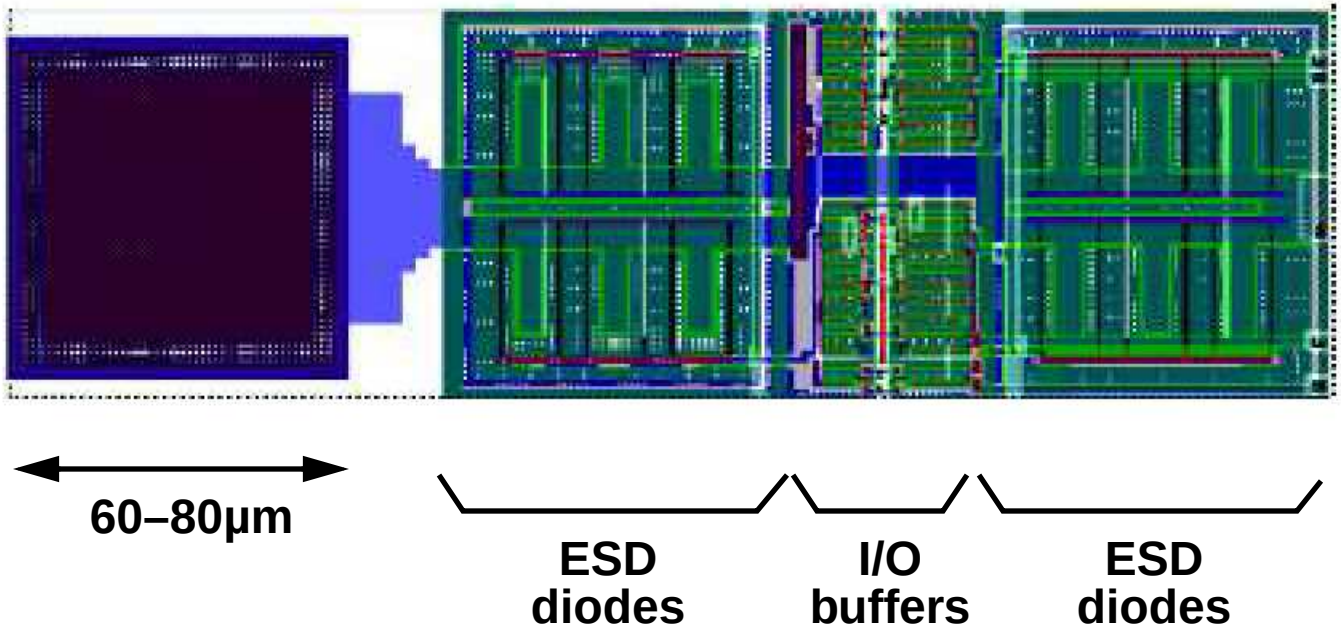
Solutions to Wire-Delay Prob.



Bus encoding to reduce “bad” transitions

I/O Pad Drivers, revisited

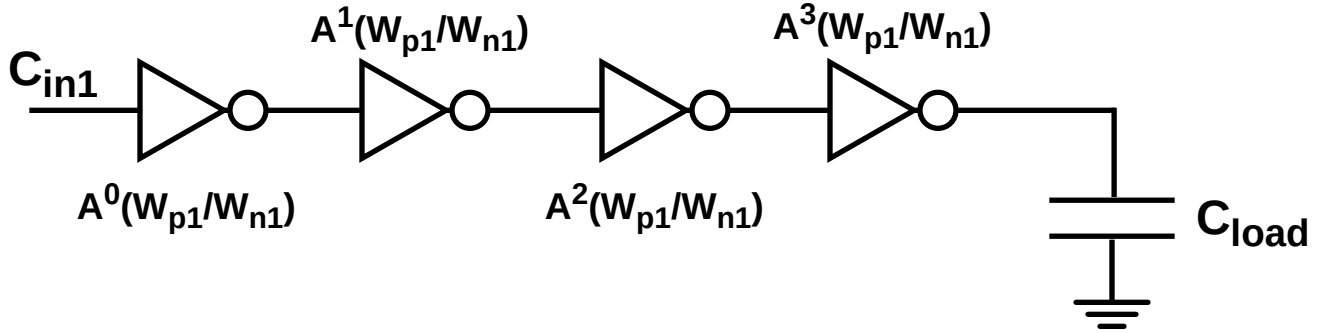


I/O Pads constrain your design:

- **Enormous capacitances, require enormous gates to drive them (plus the pins & off-chip traces)**
- ***This represents 1000x capacitive load of on-chip gate***
- **Big gates => big currents; fast clocks => small dt … VDD/VSS leads have inductance => Ldi/dt noise**

Transistor Sizing

Sizing for Large Capacitive Loads



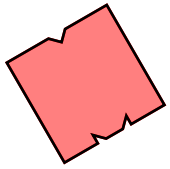
Supose C_{load} large (e.g. bond pads, etc.)

- Scale each *inverter* (both FETs in the circuit) by a factor A (input capacitances scale by A)
- If input C to last inverter * A = C_{load}
  (i.e., C_{load} looks like N+1th inverter) then we have:

$$\text{Input C of last inverter} = C_{in1}\, A^N = C_{load}$$

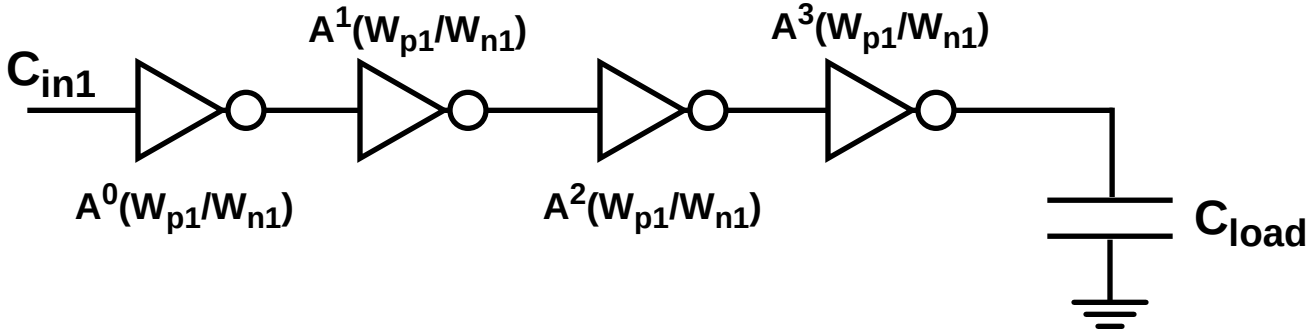
- Rearranging:

$$A = [C_{load} \div C_{in1}]^{1/N}$$



Transistor Sizing

Sizing for Large Capacitive Loads



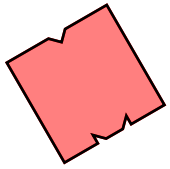
- ***Capacitances increase*** **by factor of A left to right**
- ***Resistances decrease*** **by factor of A left to right**
- **Total delay ($t_{pHL} + t_{pLH}$):**

$$(R_{n1}+R_{p1}) \bullet (C_{out1}+AC_{in1}) + (R_{n1}+R_{p1})/A \bullet (AC_{out1}+A^2C_{in1}) + \ldots$$

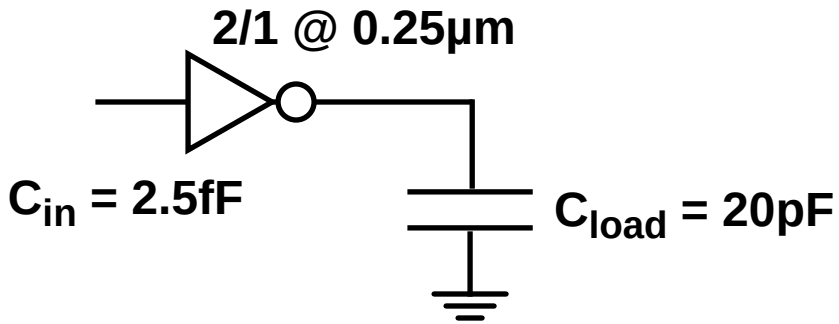
$$= N\,(R_{n1}+R_{p1}) \bullet (C_{out1}+AC_{in1})$$

- **Find optimal chain length:**

$$N_{opt} = \ln(C_{load} \div C_{in1})$$

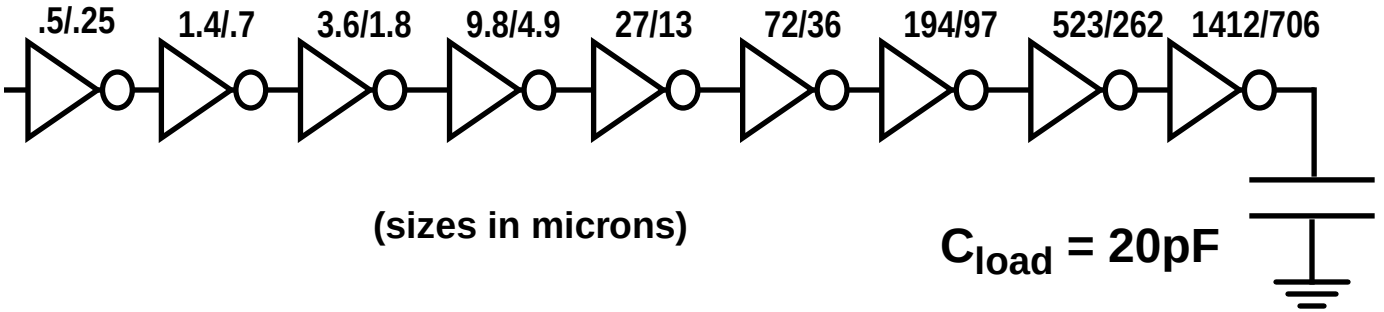


Example



Load is ~8000x that of single inverter's input capacitance: find optimal solution.

Example



$N_{opt} = \ln(20pF/2.5fF) = 8.98 \Rightarrow 9$ stages

Scaling factor $A = (20pF/2.5fF)^{1/9} = 2.7$

Total delay = $(t_{pHL} + t_{pLH})$

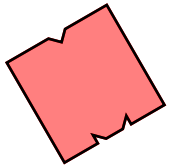
$= N (R_{n1}+R_{p1}) \bullet (C_{out1}+AC_{in1})$

$= N (R_{n1}+R_{p1}) \bullet (C_{out1} + [C_{load} \div C_{in1}]^{1/N} C_{in1})$

(assume $C_{in1} = 1.5C_{out1} = 2.5$ fF)

$= 9 \bullet (31/9 + 13/3) \bullet (1.85fF + 2.7 \bullet 2.5fF)$

= 602 ps (0.6 ns)



But Wait!

You don't (necessarily) need the optimal arrangement

You can (perhaps) get away with a slower circuit

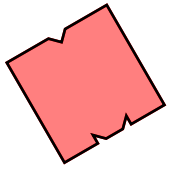
Say, for example, you want 1GHz (1ns) …

0.6ns is overkill

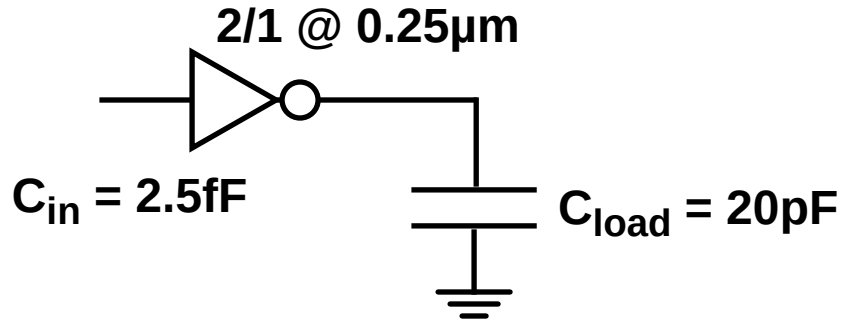
Minimize (integer) N to obey

$$\frac{t_{p,max}}{t_{p0}} \geq \ln(\text{Fan-out})\frac{A}{\ln(A)} = N \times \text{Fan-out}^{1/N}$$

(requires numerical methods)



Example, revisited



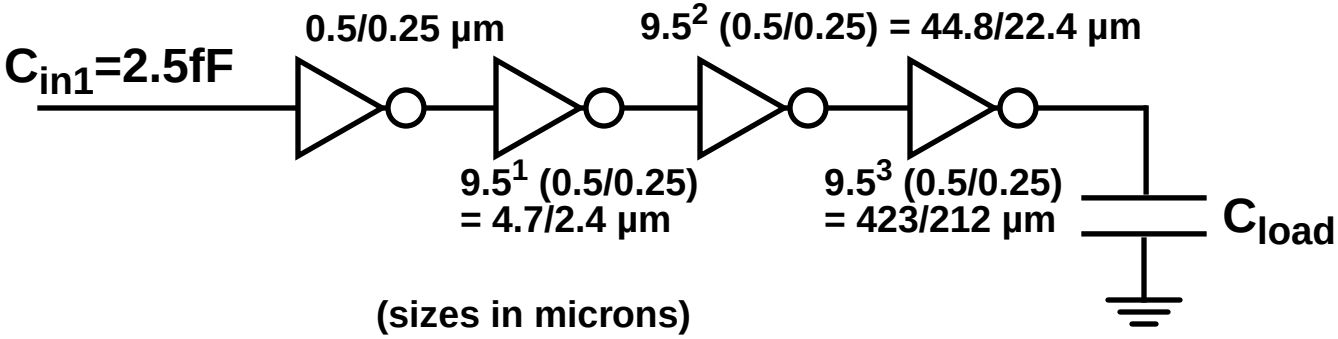
Load is ~8000x that of single inverter's input capacitance: find optimal solution.

If $t_{p,max}$ = 1ns (and not 0.6ns) we can have

N=4

Scaling factor A = $(20pF/2.5fF)^{1/4}$ = 9.46

Example, revisited



(sizes in microns)

N_{opt} => 4 stages

Scaling factor A = $(20pF/2.5fF)^{1/4}$ = 9.46

Total delay = $(t_{pHL} + t_{pLH})$

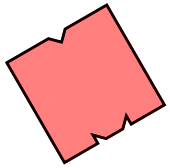
= $N (R_{n1}+R_{p1}) \bullet (C_{out1}+AC_{in1})$

= $N (R_{n1}+R_{p1}) \bullet (C_{out1} + [C_{load} \div C_{in1}]^{1/N} C_{in1})$

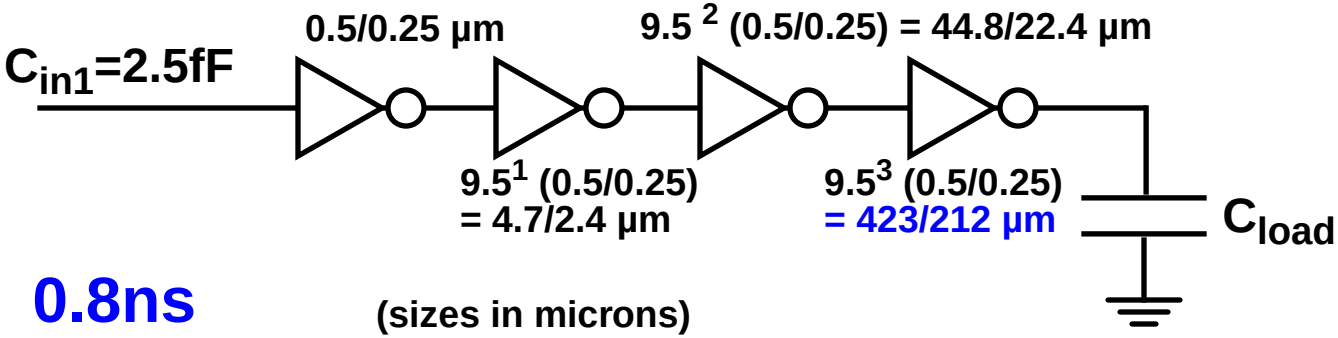
(assume $C_{in1} = 1.5C_{out1}$ = 2.5 fF)

= 4 • (31/9 + 13/3) • (1.85fF + 9.46 • 2.5fF)

= 793 ps (0.8 ns)



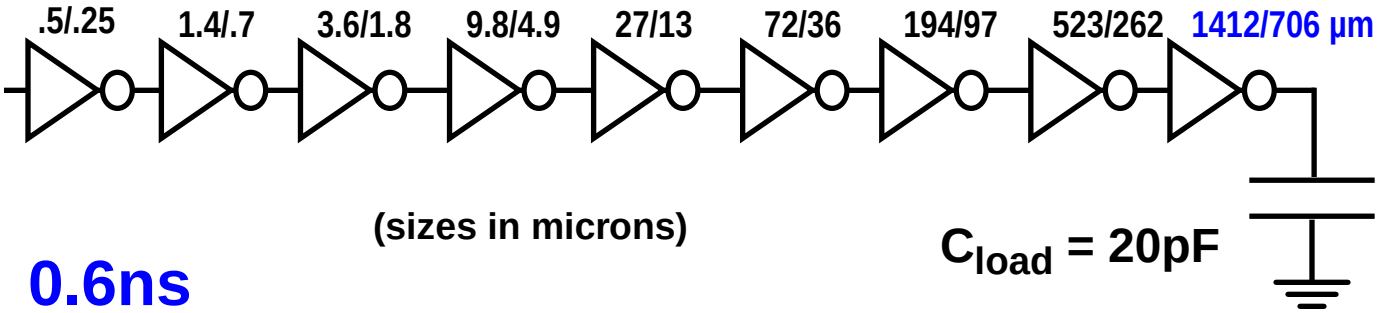
Example, revisited



0.8ns

(sizes in microns)

Versus:

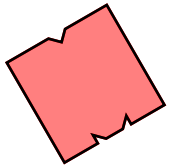


(sizes in microns)

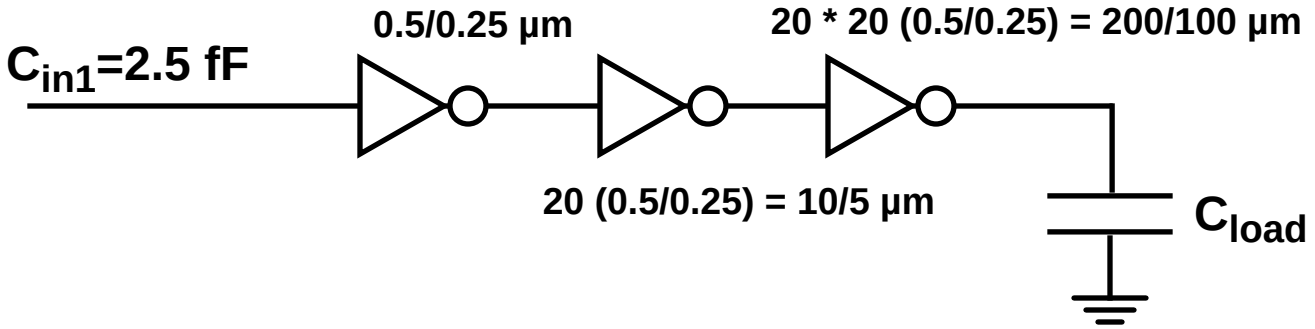
0.6ns

Reduced area, reduced current, reduced capacitance, nearly same speed

(better parasitics, ground bounce effects)



Can we do better?



N_{opt} => 3 stages

Scaling factor A = $(20pF/2.5fF)^{1/3}$ = 20

Total delay = $(t_{pHL} + t_{pLH})$

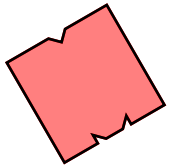
$= N (R_{n1}+R_{p1}) \bullet (C_{out1}+AC_{in1})$

$= N (R_{n1}+R_{p1}) \bullet (C_{out1} + [C_{load} \div C_{in1}]^{1/N} C_{in1})$

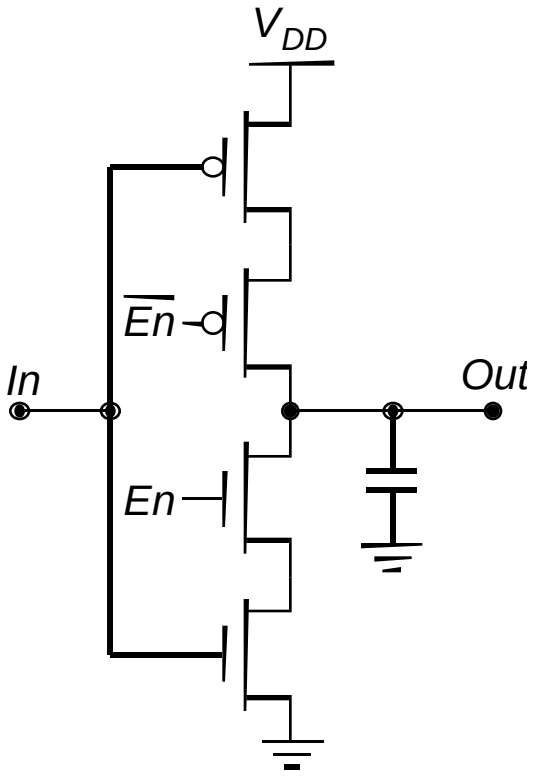
(assume $C_{in1} = 1.5C_{out1}$ = 2.5 fF)

$= 3 \bullet (31/9 + 13/3) \bullet (1.85fF + 20 \bullet 2.5fF)$

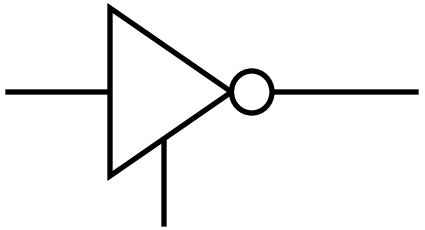
= 1210 ps (1.2 ns)

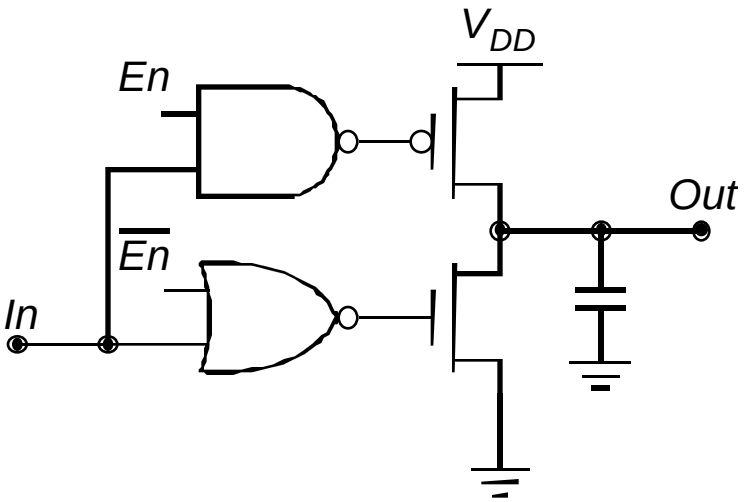


Tri-State Buffers



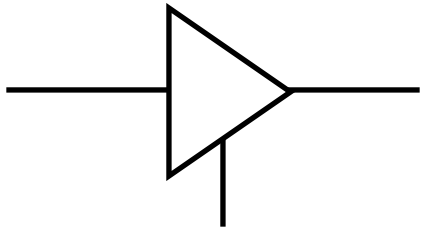
Inverting tri-state buffer

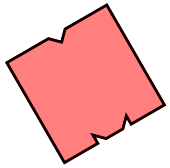




Increased output drive

Non-inverting tri-state buffer





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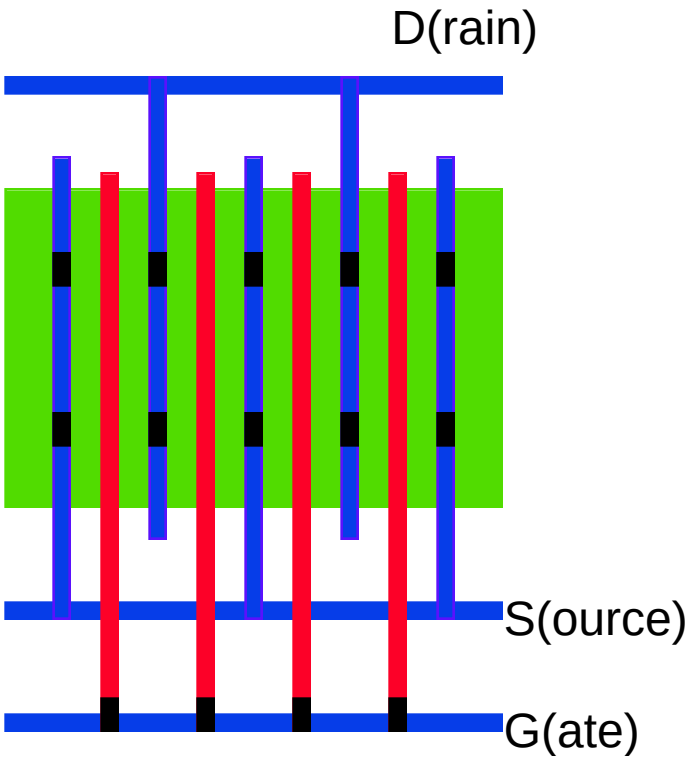
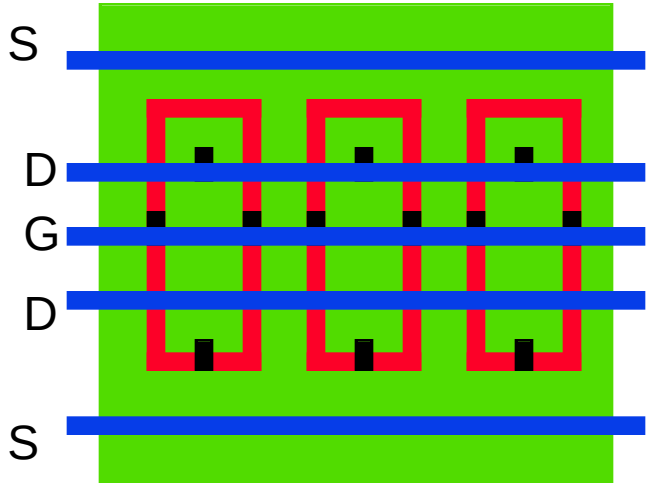
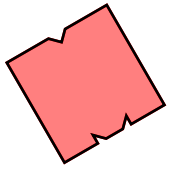
Designing Large Transistors







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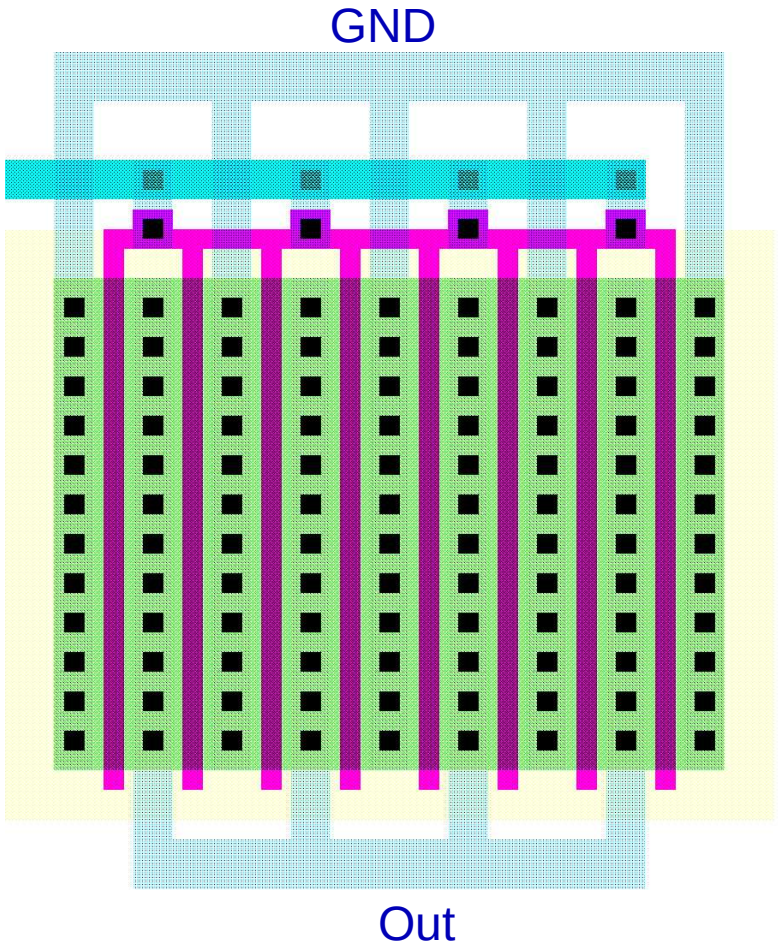
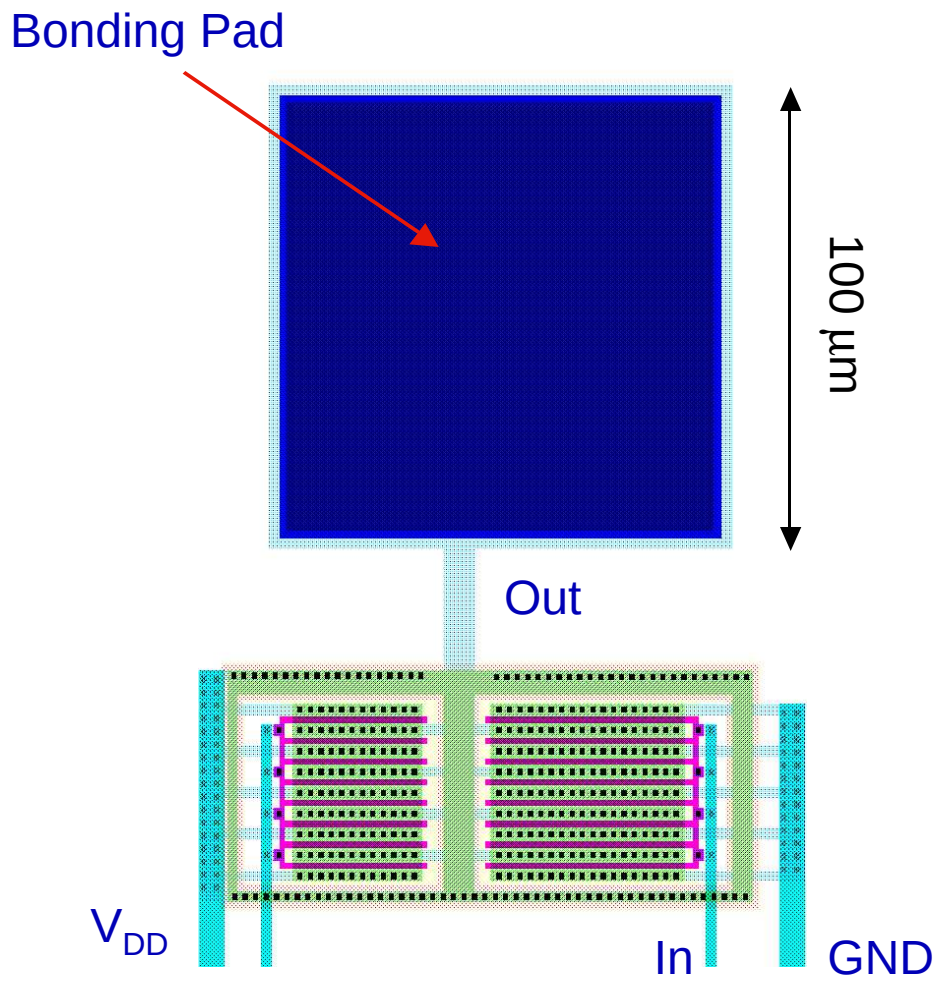
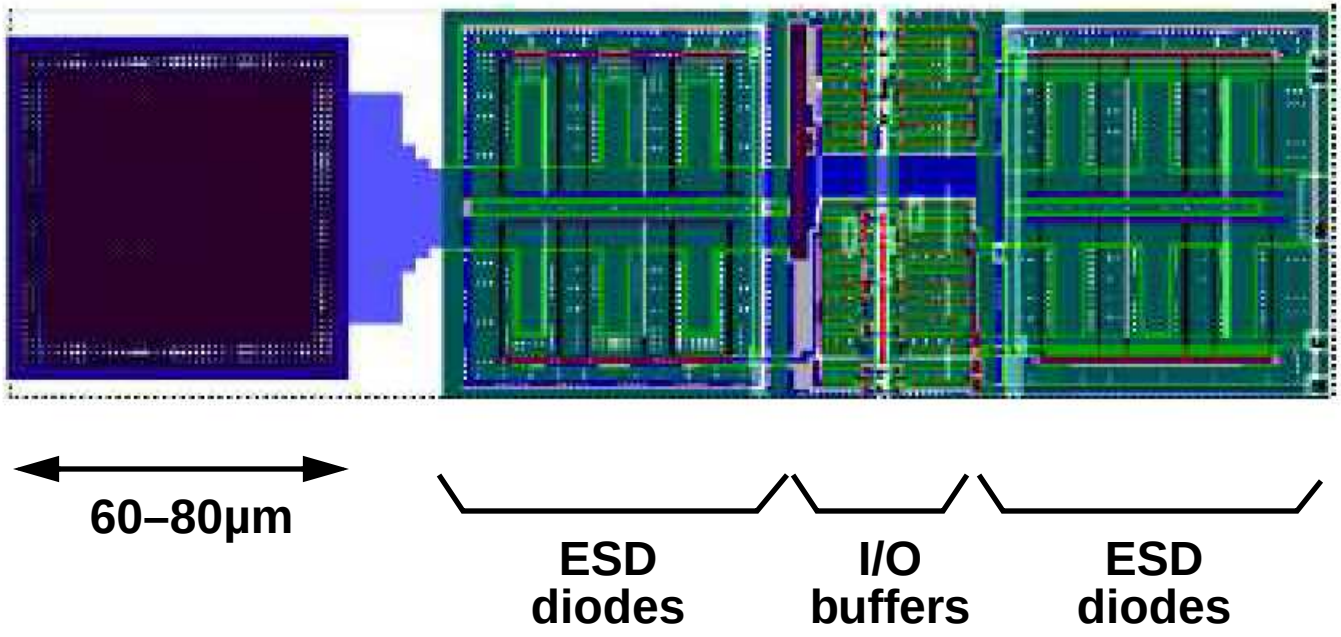


I/O Pads, again



Where have you seen this before?

I/O Pad Drivers, revisited

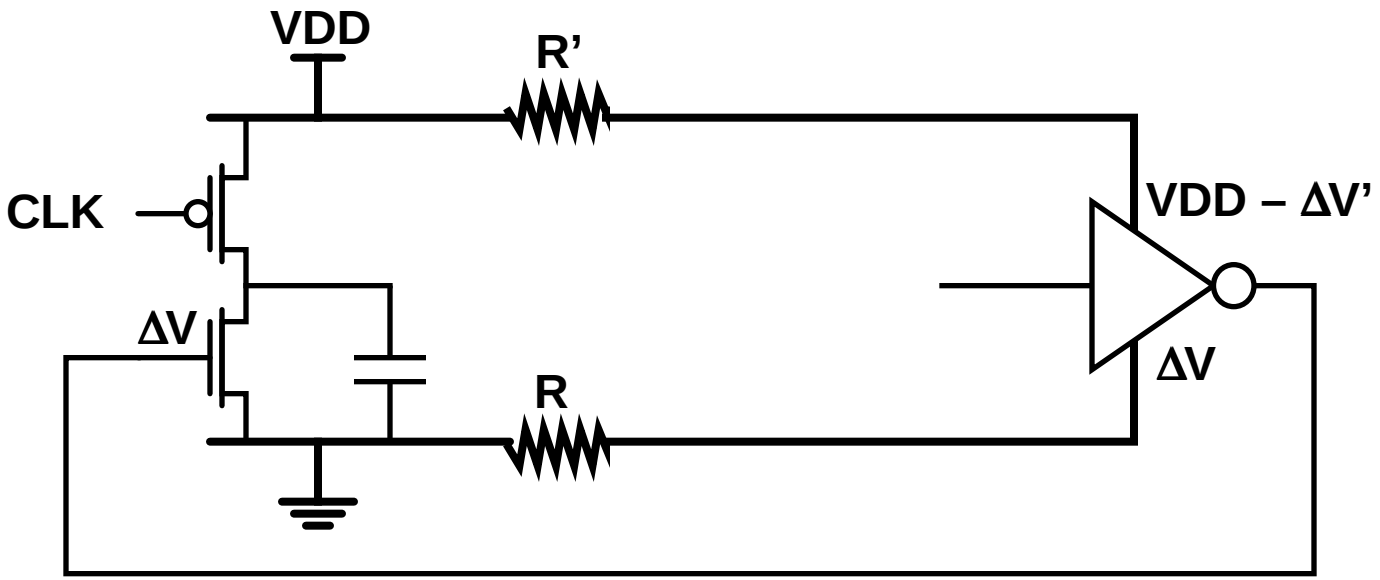


Oh yeah …

Resistive Parasitics

Basic Idea: IR drops over long distances

Power Rails



Possible to get relatively large non-zero voltage at input: reduces noise margins

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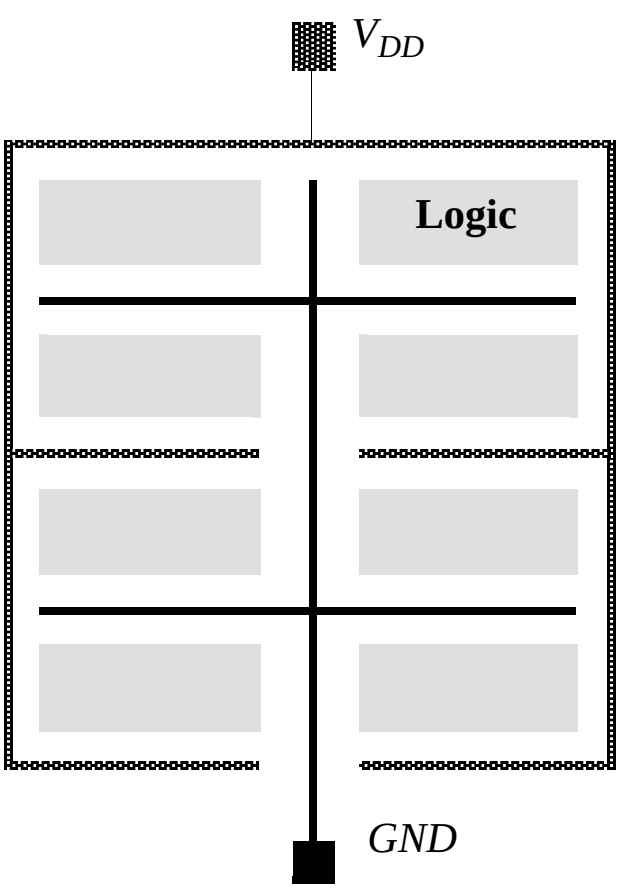
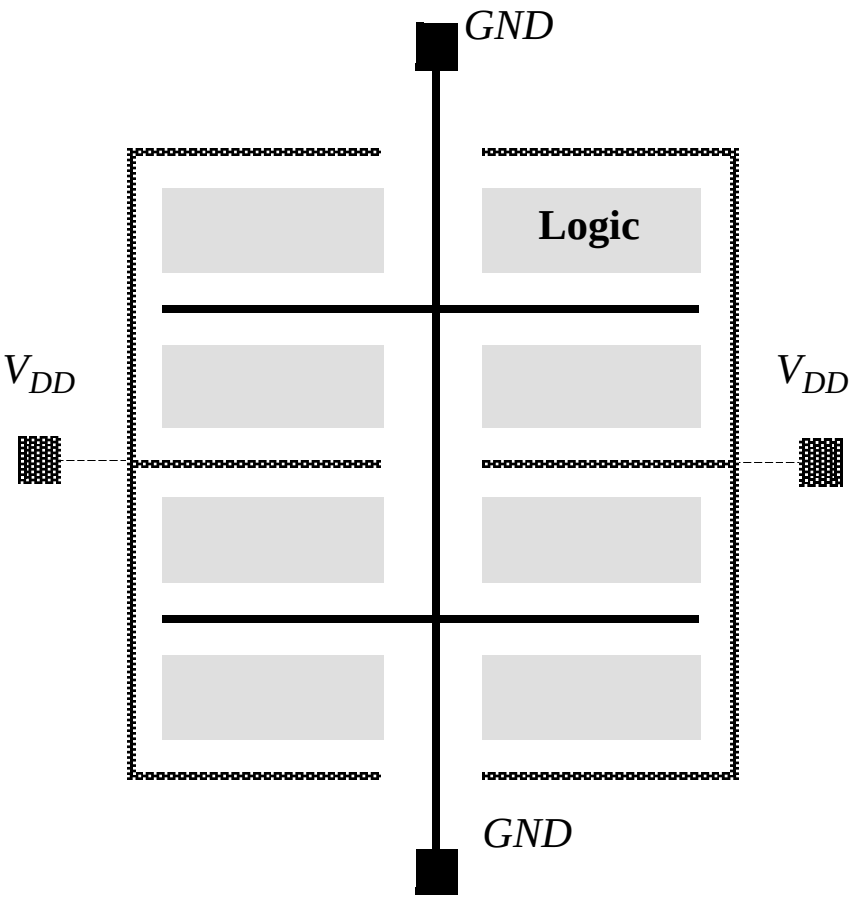
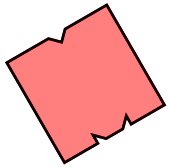
Power/Ground Distribution



(a) Finger-shaped network



(b) Network with multiple supply pins



Resistive Parasitics

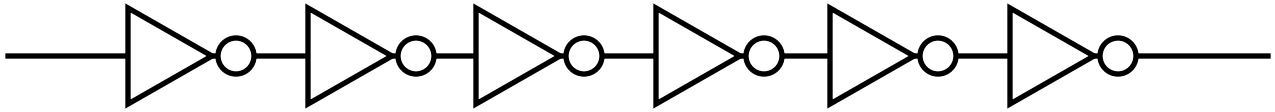
IR Drops and RC Delay over long wires

- **(remember: delay of wire is quadratic w/ its length)**

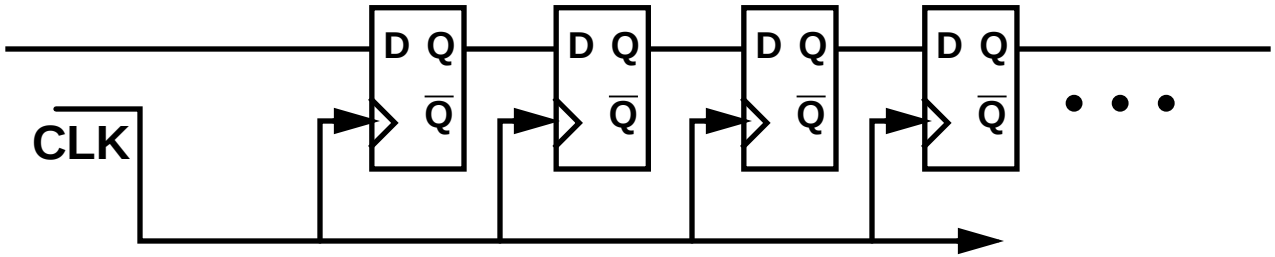
Solution: repeaters or pipelining

Instead of this:

Do this:

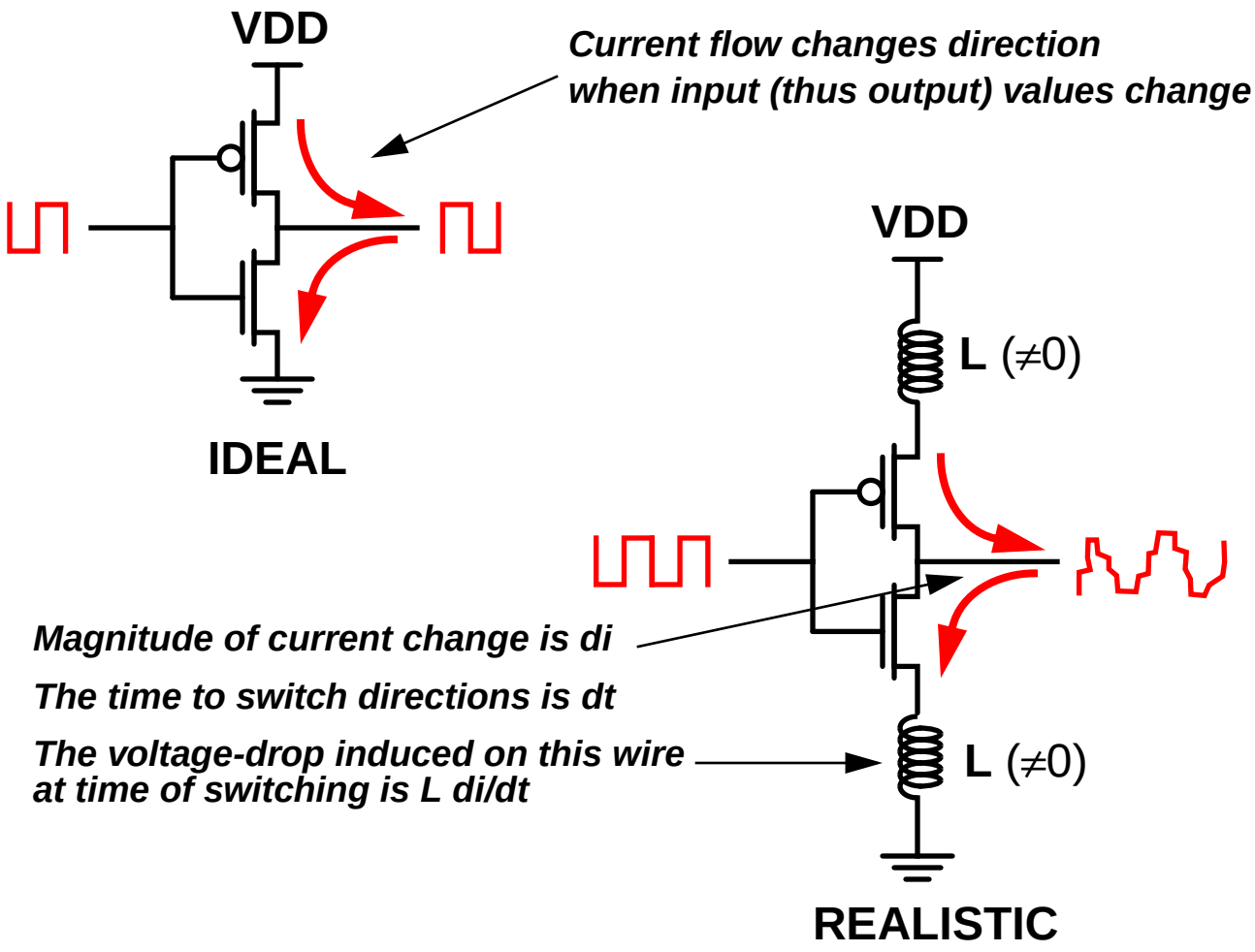


Or this:



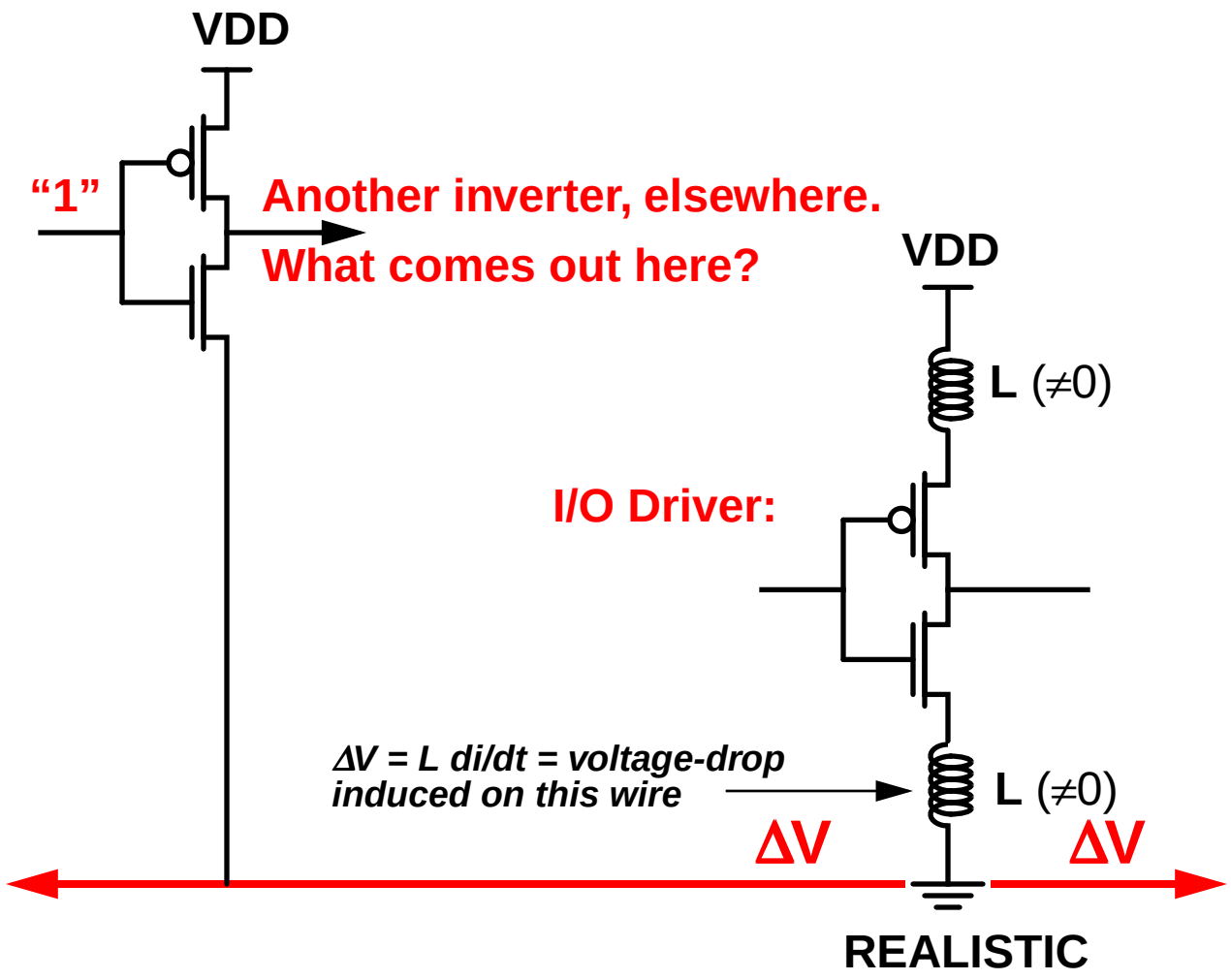
Inductive Parasitics

L di/dt noise (ground bounce):



Inductive Parasitics

L di/dt noise (ground bounce):



Inductive Parasitics

Simultaneous Switching Noise: