ENEE 359a
Digital Electronics

Interconnects

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Credit where credit is due:
Slides contain original artwork (© Jacob 2004) as well as material taken liberally from Irwin & Vijay's CSE477 slides (PSU), Schmit & Strojwas's 18-322 slides (CMU), Dally's EE273 slides (Stanford), Wolf's slides for *Modern VLSI Design*, and/or Rabaey's slides (UCB).

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Overview

- **Wires and their physical properties (MOSFETs, too …)**
- **LC/RC/RLC transmission lines, characteristic impedance, reflections**
- **Dynamic considerations (e.g. skin effect)**
- **The Bottom Line: propagation delay, transistor sizing, inductive (Ldi/dt) noise, capacitive coupling, signal degradation, various rules of thumb for design**

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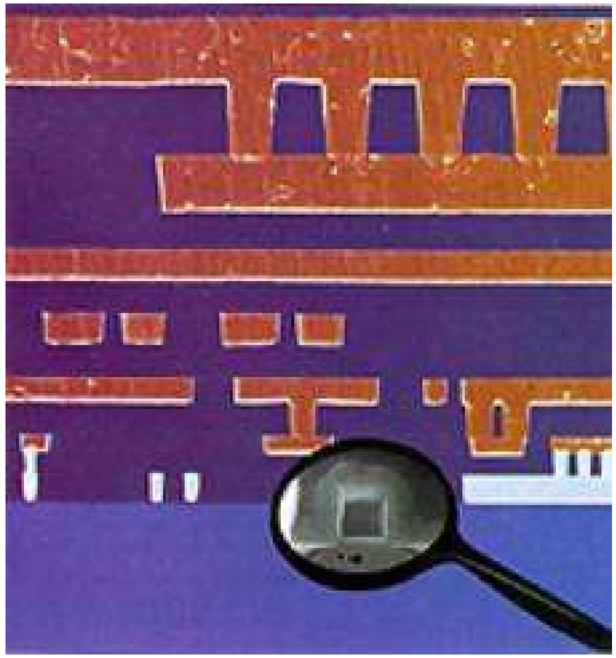
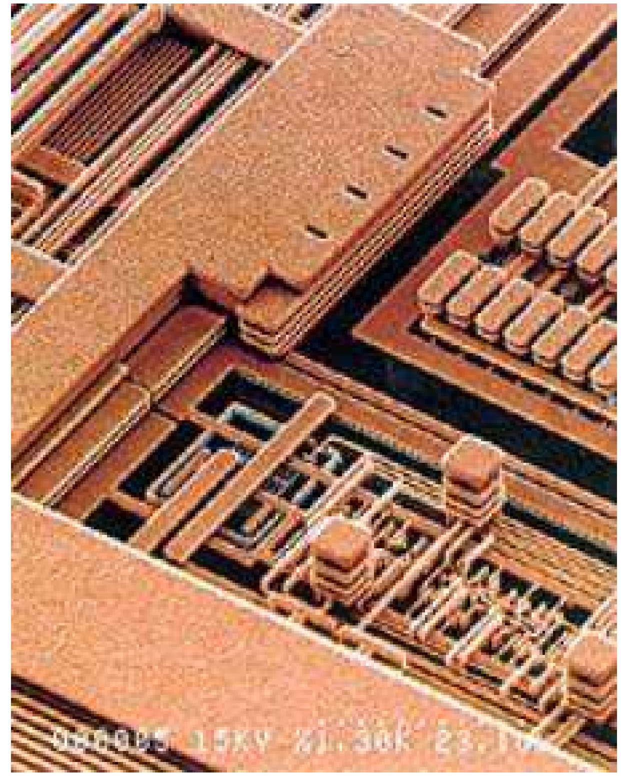
Metal Layers in ICs





IBM’s 6-layer copper interconnect

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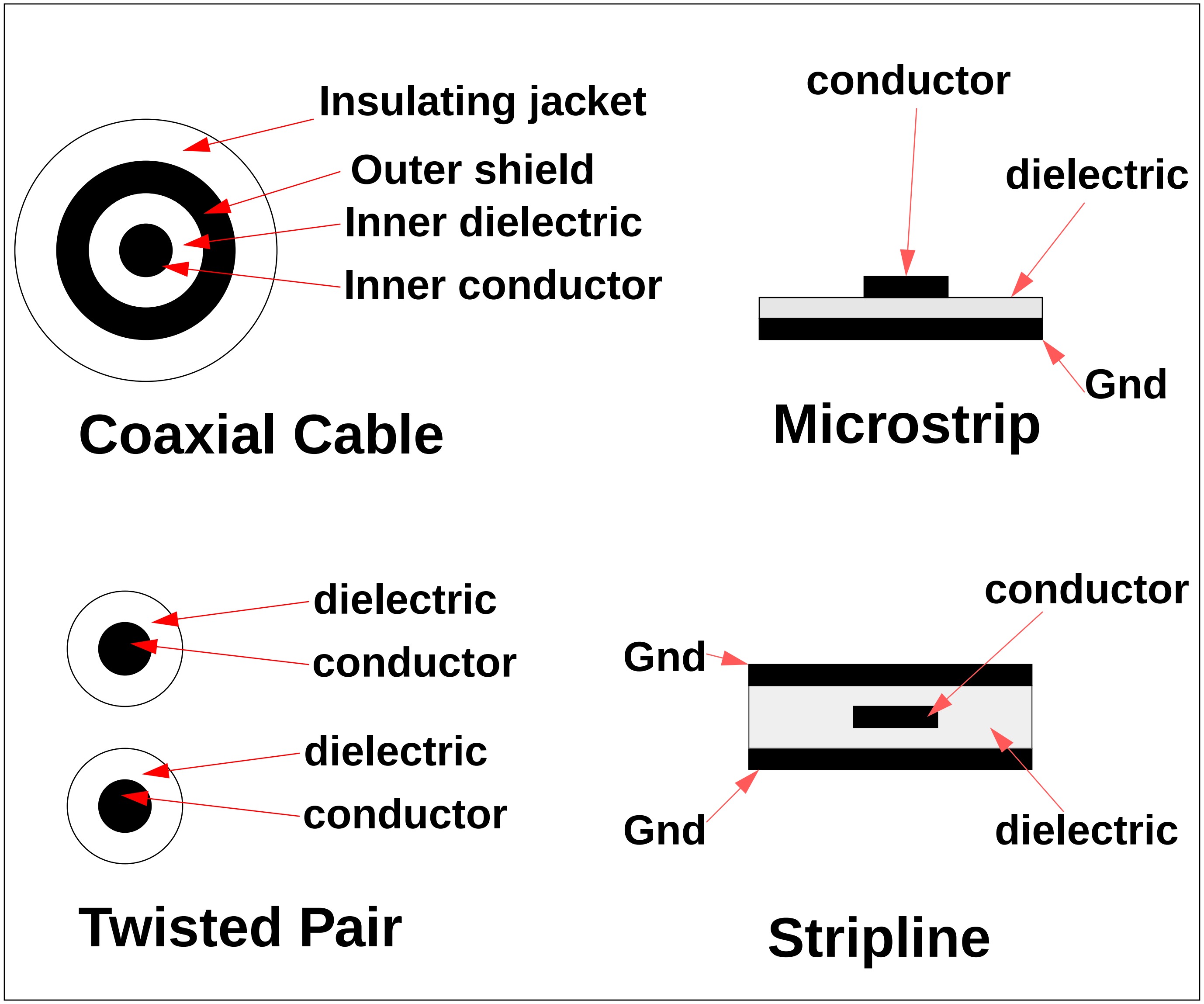
Some Transmission Lines



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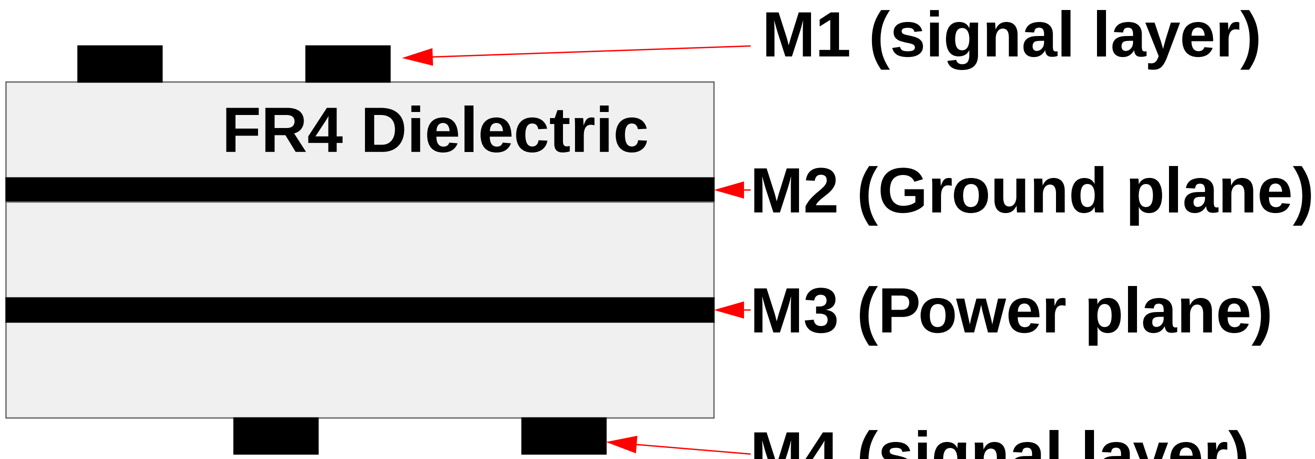
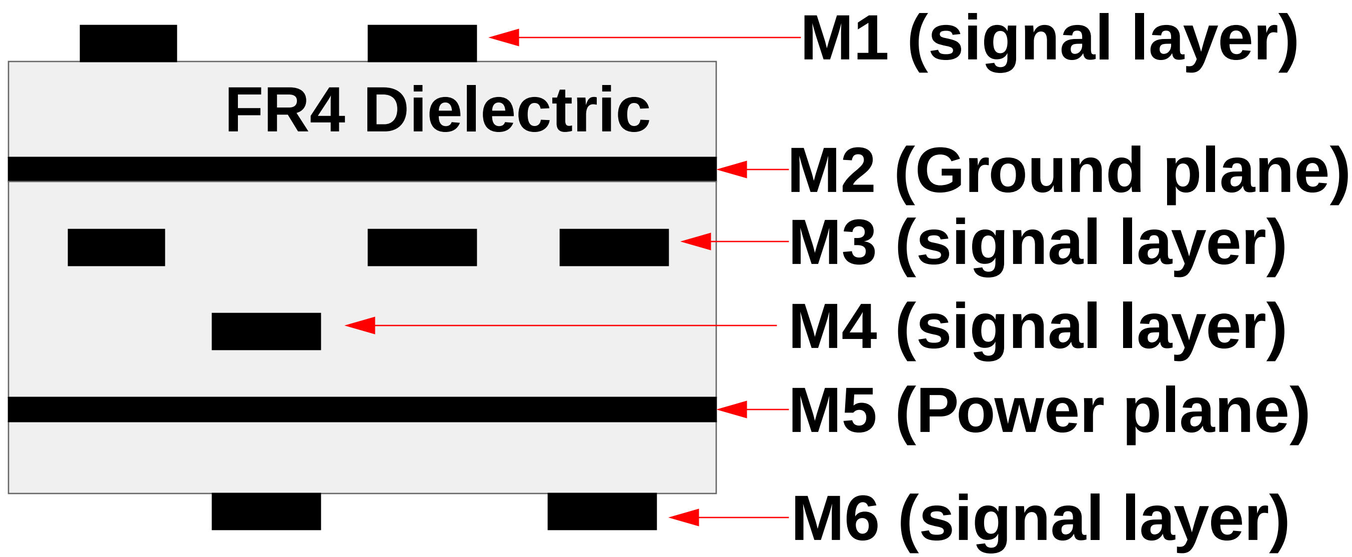
Cross Section of PCB Board





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Wires in Digital Systems

Physically, wires are

- **Stripguides on (and *in*) printed circuit-board cards, layed over & sandwiched between groundplanes**
- **Stripguides on ICs, layered atop each other**
- **Conductors in cables & cable assemblies**
- **Connectors**

We tend to treat them as *IDEAL wires*

- **No delay (equipotential)**
- **No capacitance, inductance, or resistance**

They are *NOT* ideal …

To build reliable systems, must understand properties & behavior

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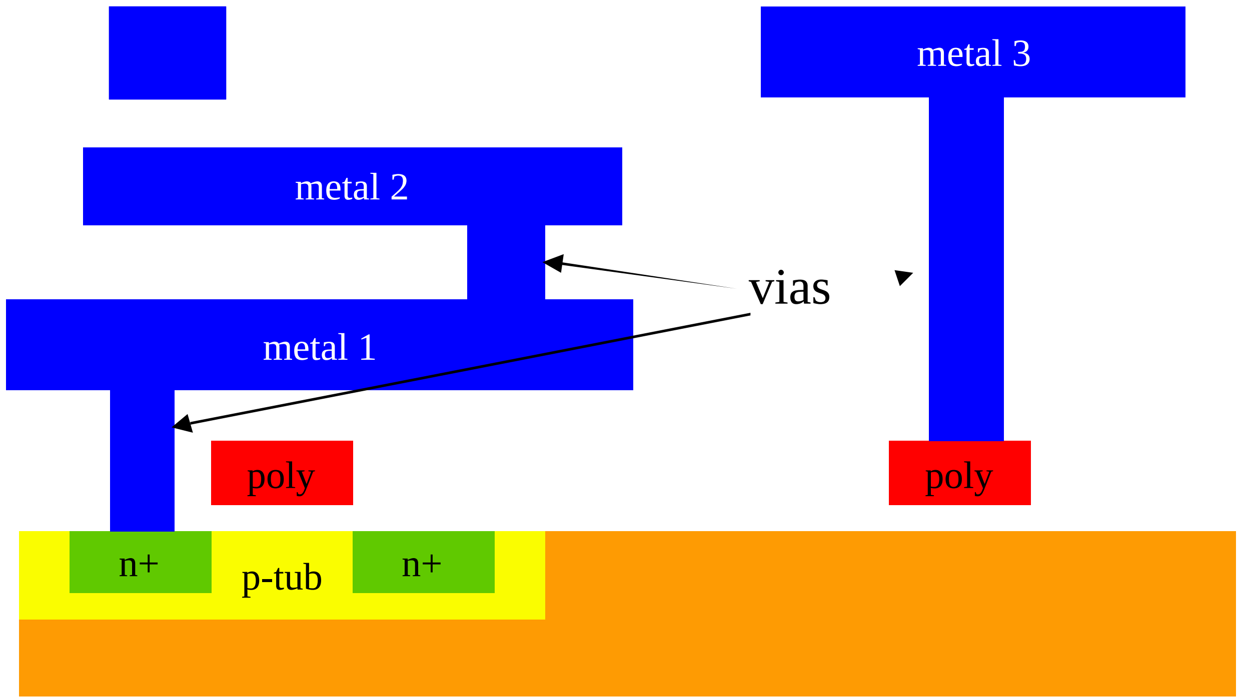
Metal Layers in ICs



Remember the *RC Constant* τ?

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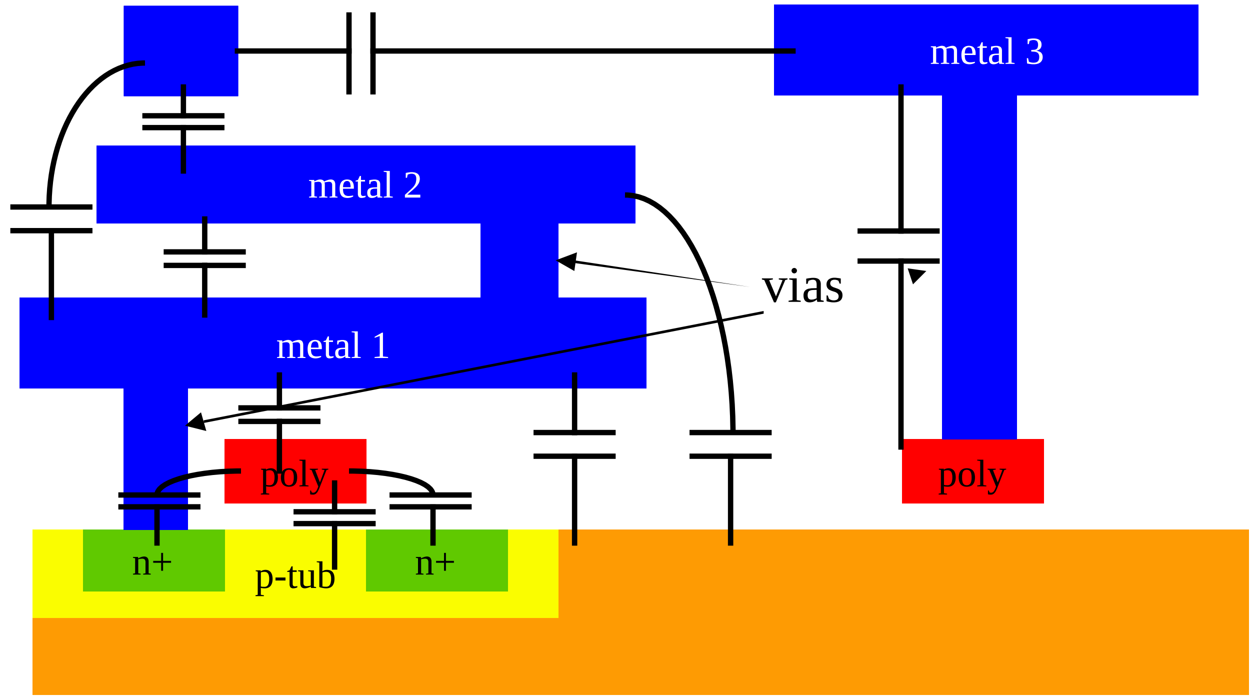
Metal Layers & Capacitances



- **On-chip wires run in multiple layers with no explicit return planes (ground is used as implicit return)**
- **Thus, almost all capacitance of on-chip wire is to *other wires* (same plane, different plane, etc.)**
- **Capacitance of MOSFET scales with Vdd**

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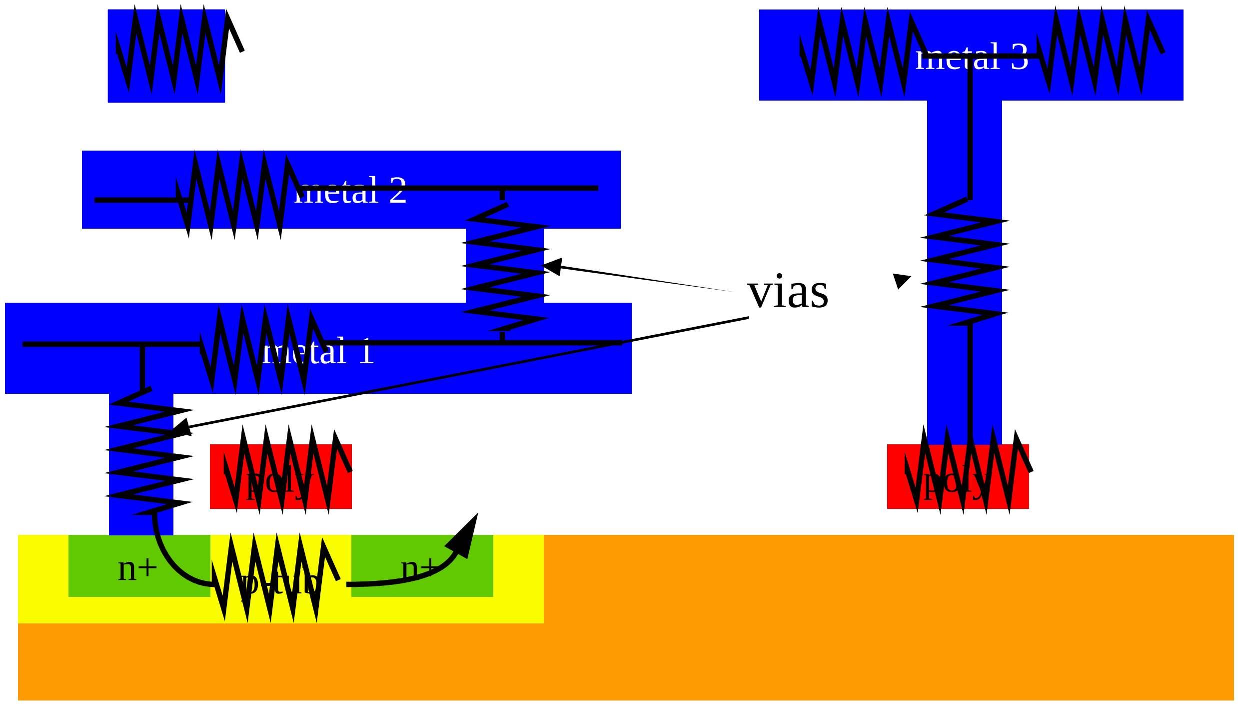
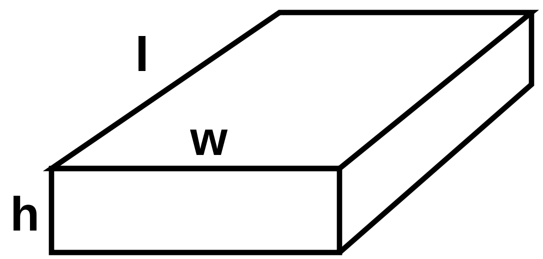
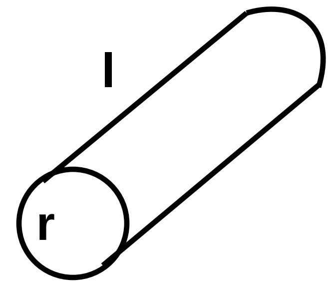
Metal Layers & Resistances



- **Resistance of conductor proportional to length/width, depends on material (resistivity), causes delay & loss**
- **Resistance of wire scales with square root of signaling frequency (at high speeds) ("skin effect")**
- **Process scaling tends to increase resistance**

Wire Resistance





- **$R = \rho l/A = \rho l/(wh)$ for rectangular wires (on-chip wires & vias, PCB traces)**
- **$R = \rho l/A = \rho l/(\pi r^2)$ for circular wires (off-chip, off-PCB)**

Material	**Resistivity ρ (Ω-m)**
Silver (Ag)	1.6 x 10-8
Copper (Cu)	1.7 x 10-8
Gold (Au)	2.2 x 10-8
Aluminum (Al)	2.7 x 10-8
Tungsten (W)	5.5 x 10-8

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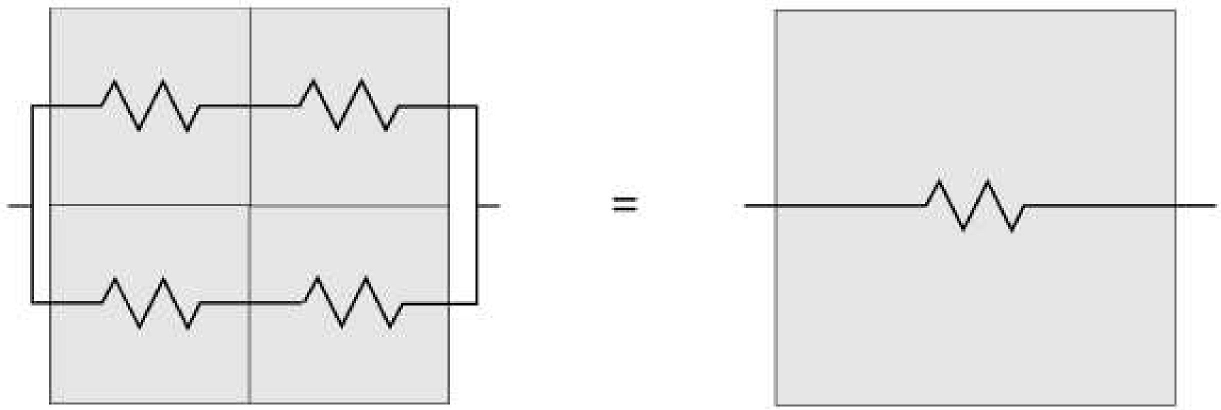
Sheet Resistance



$R = \rho l/(wh) = l/w \cdot \rho/h$ for rectangular wires

Sheet resistance $R_{sq} = \rho/h$

Material	**Sheet resistance R_{sq} (Ω/sq)**
n, p well diffusion	1000 to 1500
n+, p+ diffusion	50 to 150
polysilicon	150 to 200
polysilicon with silicide	4 to 5
Aluminum	0.05 to 0.1

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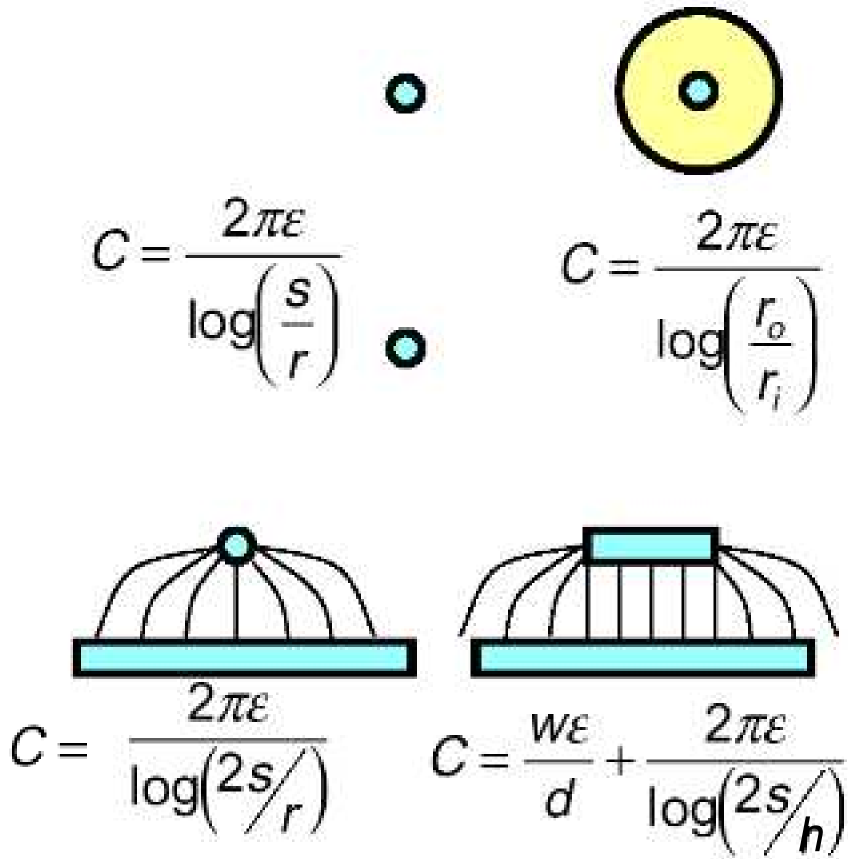
Wire Capacitance

Common wire cross-sections/permittivities:



Material	ε_r
Air	1
Teflon	2
Polymide	3
SiO_2	3.9
Glass-epoxy (PCB)	4
Alumina	10
Silicon	11.7

- **Permittivity $\varepsilon = \varepsilon_0 \varepsilon_r$**
- **Permittivity of free space $\varepsilon_0 = 8.854 \times 10^{-12}$ F/m**

Inductance

When conductors of transmission line are surrounded by uniform dielectric, capacitance & inductance are related:

$$CL = \varepsilon\mu$$

Inductive effects can be ignored

- if the resistance of the wire is substantial enough (as is the case for long Al wires with small cross section)
- if rise & fall times of applied signals are slow enough

So … inductance must be considered

- for off-chip signals (even power/ground)
- for future even-higher-speed on-chip signalling

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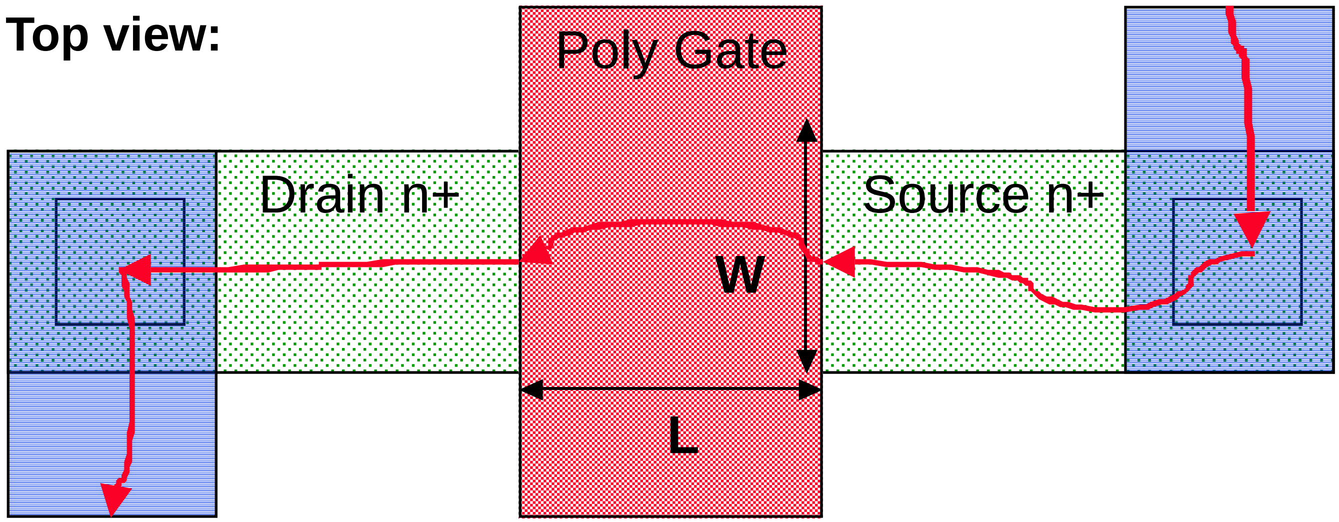
MOSFET Resistance

Top view:



- **MOS structure resistance - R_{on}**
- **Source and drain resistance**
- **Contact (via) resistance**
- **Wiring resistance**

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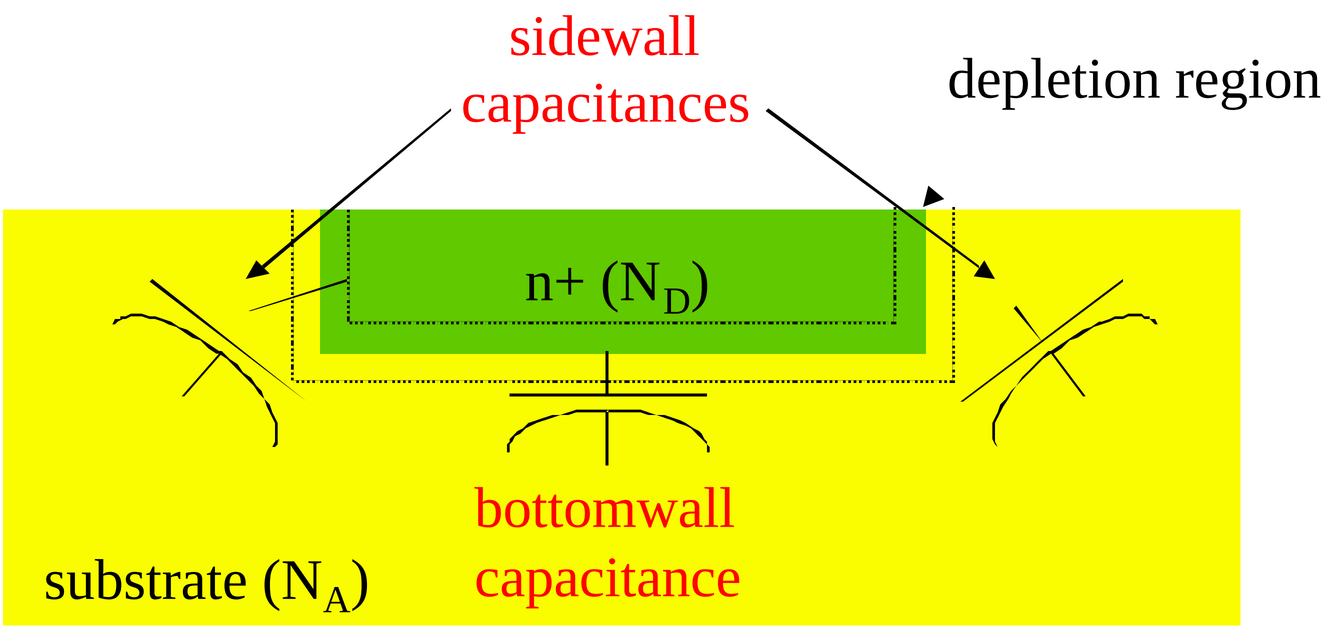
MOSFET Capacitance



Capacitances formed by p/n junctions

Depletion-region capacitances *decrease* with voltage across region; resistances *increase* with voltage across region

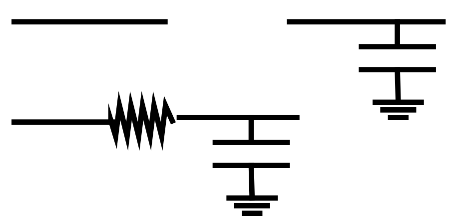
Wires & Models

Example Wires:

Type	W	R	C	L
On-chip	0.6 µm	150k Ω/m	200 pf/m	600 nH/m
PC Board	150 µm	5 Ω/m	100 pf/m	300 nH/m
24AWG pair	511 µm	0.08 Ω/m	40 pf/m	400 nH/m

In a situation, use a *model* of wires that captures the properties we need:

- **ideal, lumped L, R, or C**
- **LC, RC, RLC transmission line**
- **General LRCG transmission line**



Appropriate choice of model depends on signaling frequency

$$f_0 = \frac{R}{2\pi L}$$

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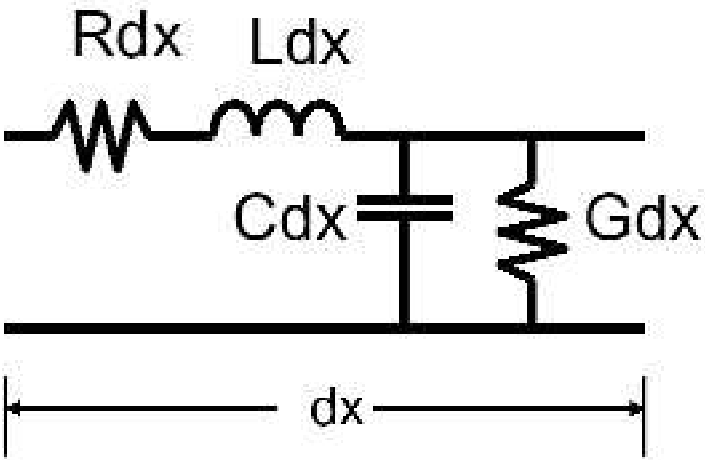
General LRCG Model

Model an *infinitesimal* length of wire, dx, with lumped components
L, R, C, and G
(inductance, resistance, capacitance, and conductance)



Drop across R and L $$\frac{\partial V}{\partial x} = RI + L\frac{\partial I}{\partial t}$$

Current into C and G $$\frac{\partial I}{\partial x} = GV + C\frac{\partial V}{\partial t}$$

$$\frac{\partial^2 V}{\partial x^2} = RGV + (RC + LG)\frac{\partial V}{\partial t} + LC\frac{\partial^2 V}{\partial t^2}$$

For G=0: $$\frac{\partial^2 V}{\partial x^2} = RC\frac{\partial V}{\partial t} + LC\frac{\partial^2 V}{\partial t^2}$$

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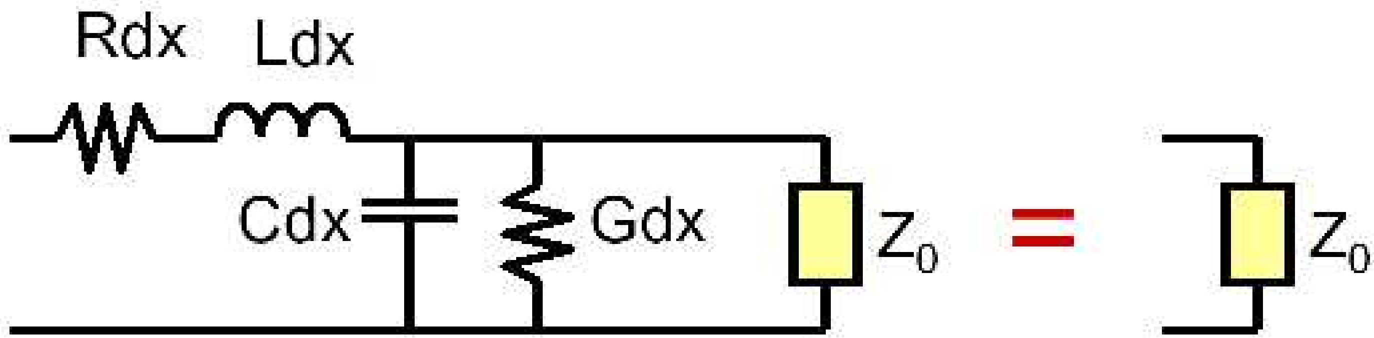
Impedance



$$Z_0 = \left(\frac{R + Ls}{G + Cs} \right)^{\frac{1}{2}} \qquad s = 2\pi j f = j\omega \qquad Z_0 = \left(\frac{L}{C} \right)^{\frac{1}{2}}$$

(typical assumption: G = 0)

At high frequency (LC lines)

- **An infinite length of LRCG transmission line has *impedance Z_0***
- **Driving a line *terminated* into Z_0 is same as driving Z_0**
- **In general, Z_0 is complex and frequency-dependent**
- **For LC lines (operating at "high" frequencies), Z_0 is real-valued and independent of frequency**

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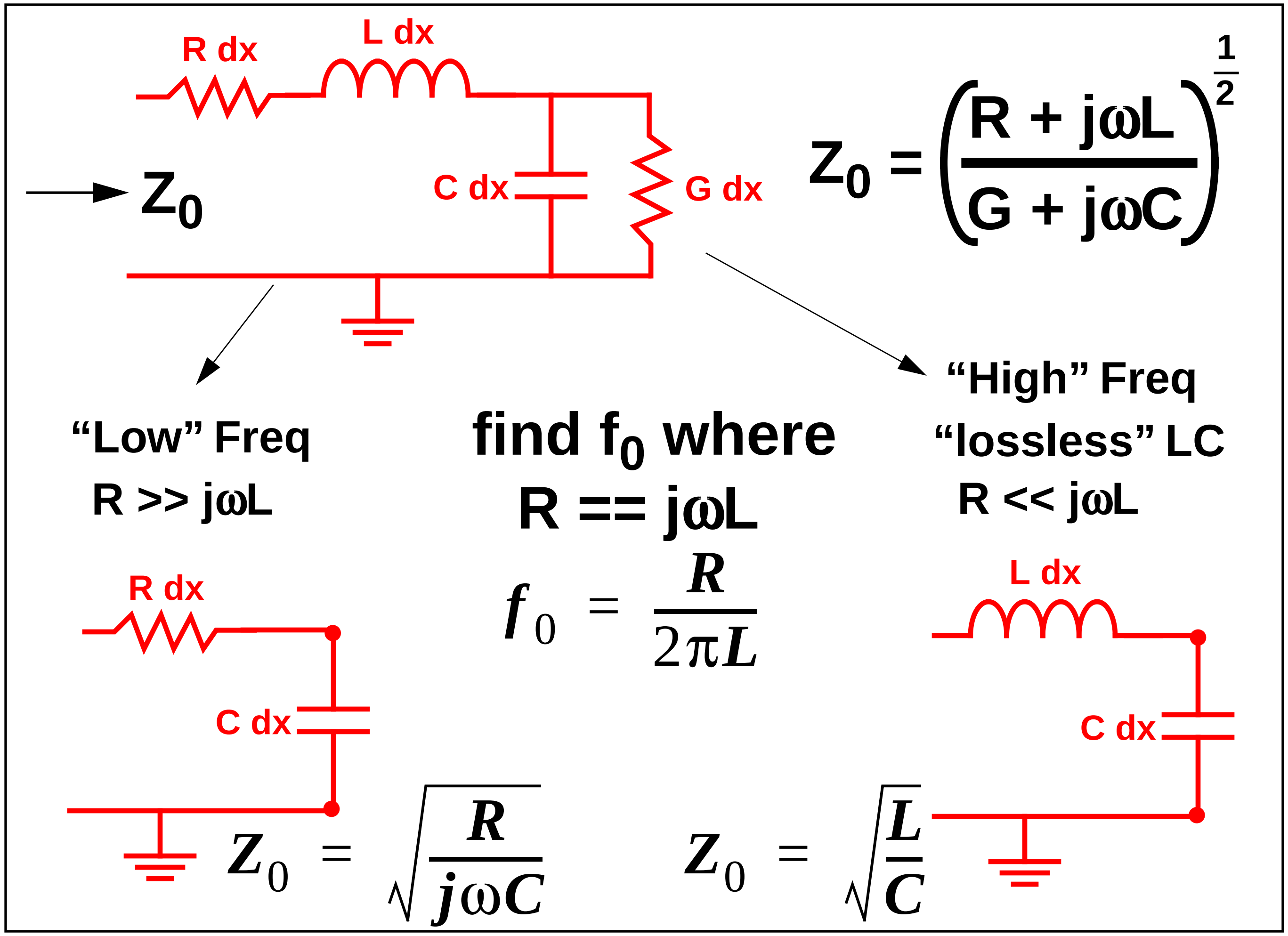
Cut-off Frequency f_0



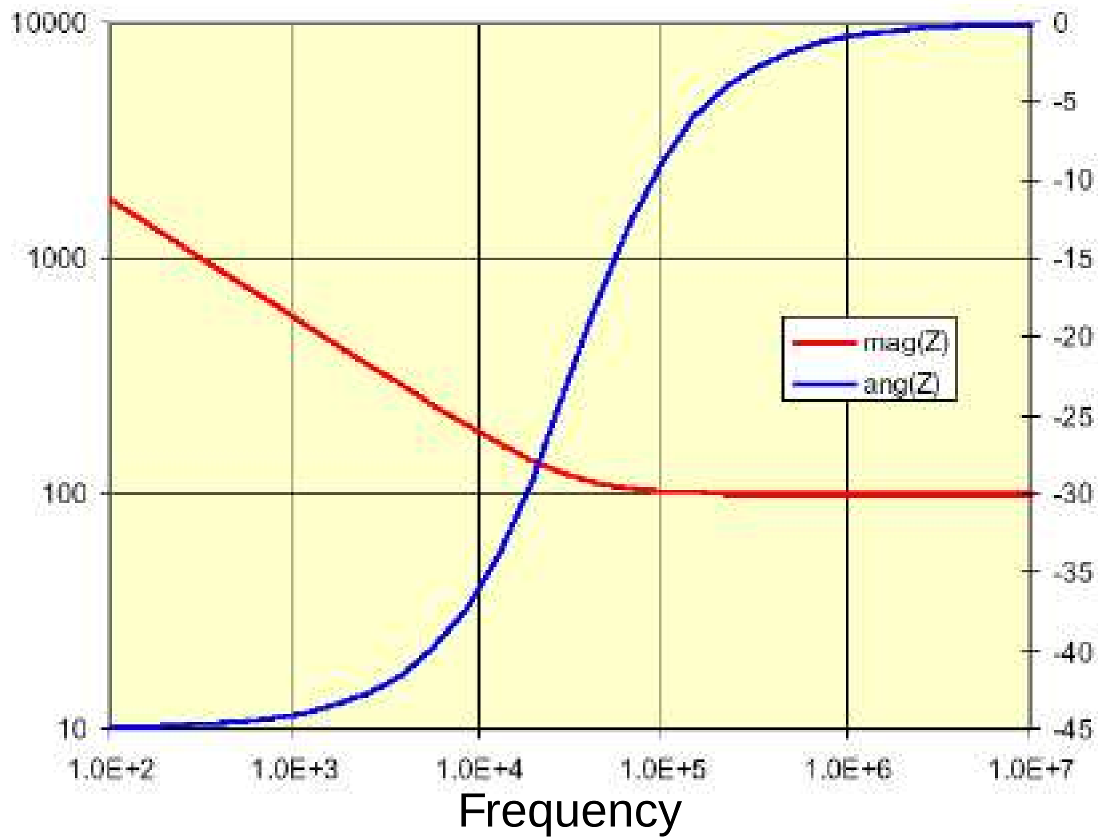
- Transmission lines have characteristic frequency f_0
- Below $f_0 \approx$ RC model, Above $f_0 \approx$ LC model

Cut-off Frequency f_0

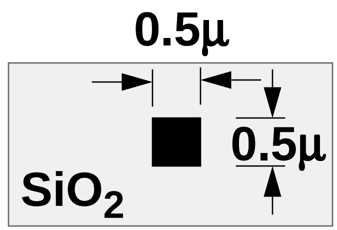
Example, 24AWG Pair

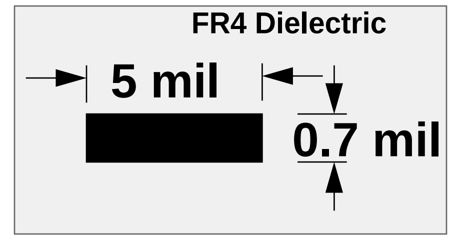
- f_0 = 33kHz
- Below f_0, line is RC
- Above f_0, line is LC

$$Z_0 = \left(\frac{.08 + 400 \times 10^{-9} \times 2\pi f j}{40 \times 10^{-9} \times 2\pi f j} \right)^{\frac{1}{2}}$$



Cut-off Frequency f_0 II





L = 0.6 nH/mm
C = 73 nF/mm
R_{dc} = 120Ω /mm
f_0 = 32 GHz

L = 0.5 nH/mm
C = 104 fF/mm
R_{dc} = 0.008Ω /mm
f_0 = 2.5 MHz

~RC Model for on chip interconnects

~LC Model for PC Board traces

$$Z_0 = \left(\frac{L}{C}\right)^{\frac{1}{2}} = \left(\frac{0.5\ \text{nH}}{0.1\ \text{pF}}\right)^{\frac{1}{2}} \approx 70\ \Omega$$

1 mil = 0.001 inch

Example from Poulton 1999 ISSCC Tutorial

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SLIDE 22

RC Lines (low frequency)

$$\frac{\partial^2 V}{\partial x^2} = RGV + (RC + LG)\frac{\partial V}{\partial t} + LC\frac{\partial^2 V}{\partial t^2}$$

R >> jωL, governed by diffusion equation:

$$\frac{\partial^2 V}{\partial x^2} = RC\frac{\partial V}{\partial t}$$

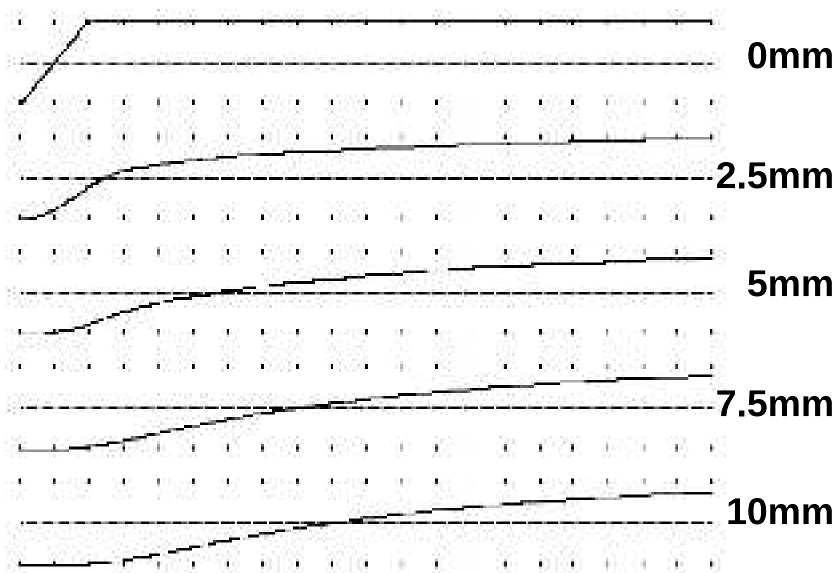
Signal diffuses down line, disperses:

R increases w/ length d

C increases with d

Delay & rise time both increase with RC, thus with d^2

For a typical wire:
- **R = 150KΩ/m**
- **C = 200pF/m**
- **τ = RC = 30 μs/m^2**
- **= 30 ps/mm^2**



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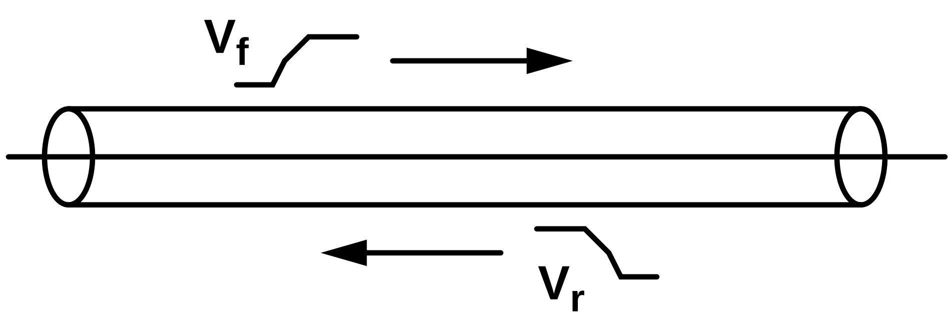
LC Lines (high frequency)

$$\frac{\partial^2 V}{\partial x^2} = RGV + (RC + LG)\frac{\partial V}{\partial t} + LC\frac{\partial^2 V}{\partial t^2}$$

R << jωL, governed by wave equation:

$$\frac{\partial^2 V}{\partial x^2} = LC\frac{\partial^2 V}{\partial t^2} \qquad V_i(x, t) = \left(\frac{Z_0}{Z_0 + R_S}\right)V_S\left(t - \frac{x}{v}\right)$$

Waveform on line is superposition of forward- and reverse-traveling waves:



- **Waves travel with velocity v = $(LC)^{-1/2}$**
- **What happens when the wave gets to the end of line?**

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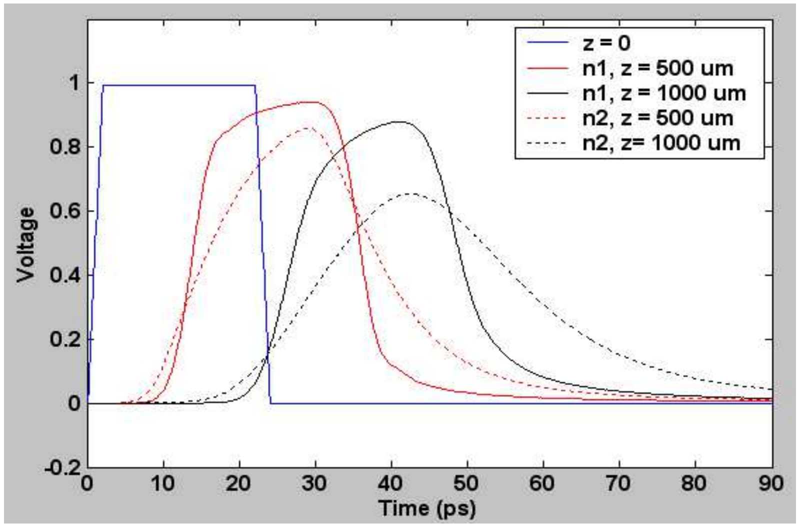
RLC/G Lines (general case)

$$\frac{\partial^2 V}{\partial x^2} = RGV + (RC + LG)\frac{\partial V}{\partial t} + LC\frac{\partial^2 V}{\partial t^2}$$

Ignoring G, wave propagation equation:

$$\frac{\partial^2 V}{\partial x^2} = RC\frac{\partial V}{\partial t} + LC\frac{\partial^2 V}{\partial t^2}$$

Lossy transmission line, dispersive waves:



Substrate-doping-dependent dispersion of a picosecond-scale pulse in propagation of an on-chip transmission line

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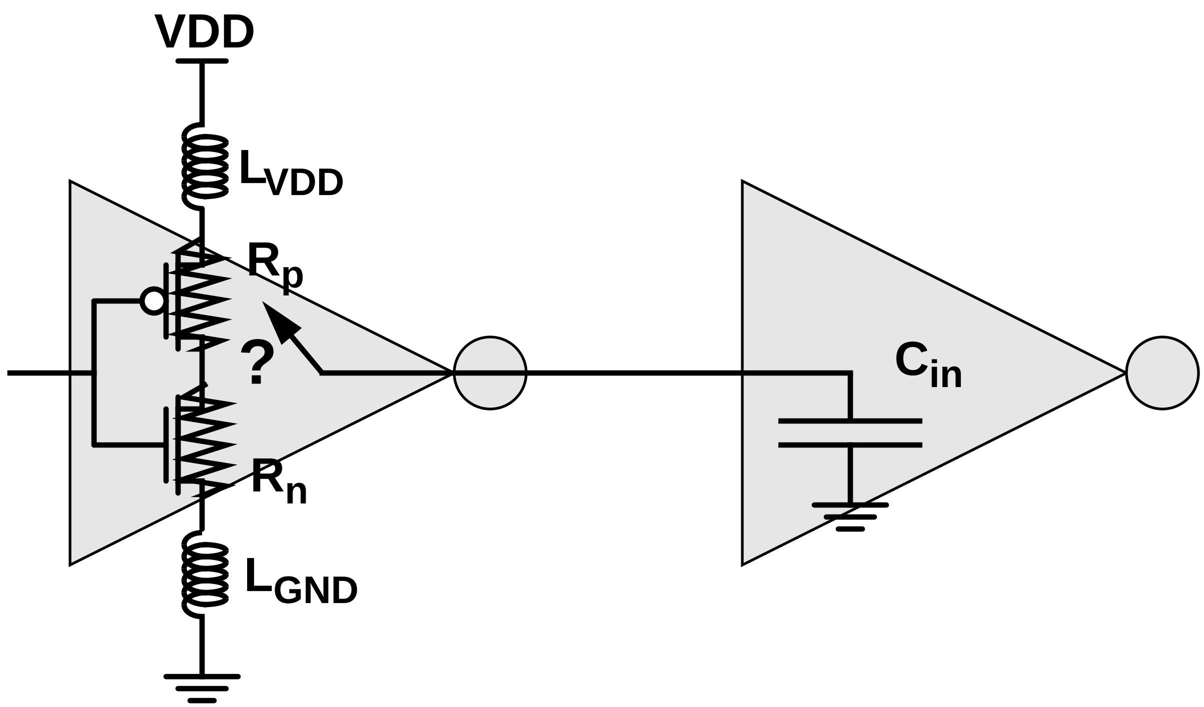
RC vs. RLC

Output response of inverter with step input:



In reality, we have a non-zero inductance in series with the RC circuit. (Inductors and capacitors both "have memory")

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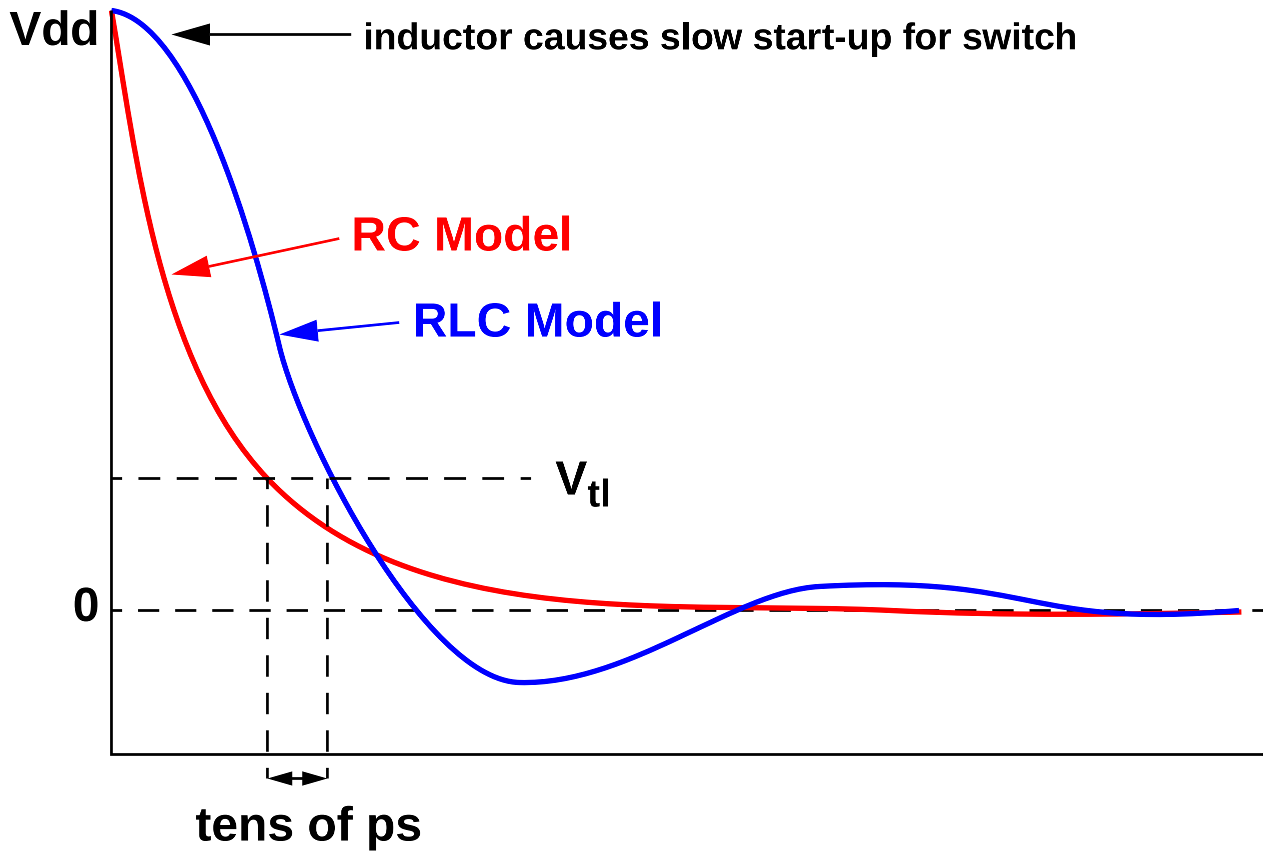
RC vs. RLC

Output response of inverter with step input:



Result: slower reponse time, ringing

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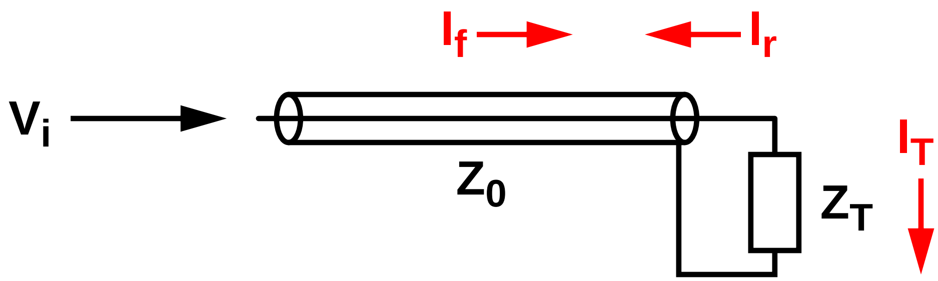
Impedance and Reflections

Terminating a Transmission Line:



Telegrapher's Equations:

$$k_r = \frac{I_r}{I_i} = \frac{V_r}{V_i} = \frac{Z_T - Z_0}{Z_T + Z_0}$$

Reflection coefficient k_r may be complex for complex impedances Z_T — i.e., the reflected wave may be phase-shifted from the incident wave.

For real-valued Z_T the reflection coefficient is real, and the phase shift is either 0 (k_r positive) or π (k_r negative).

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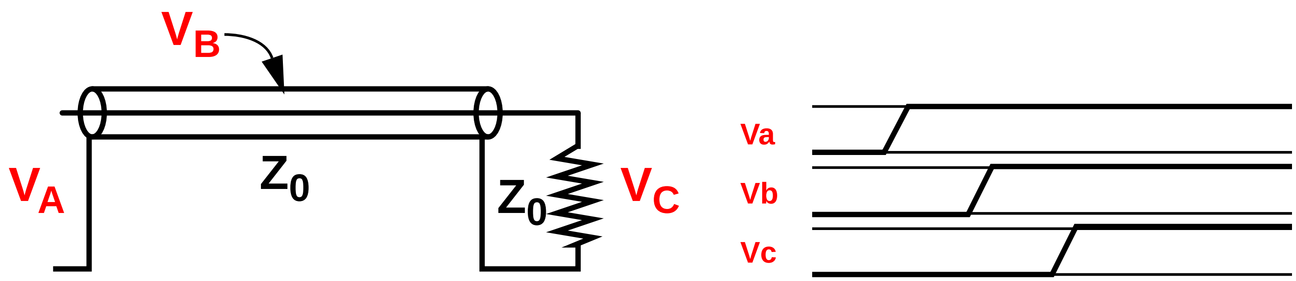
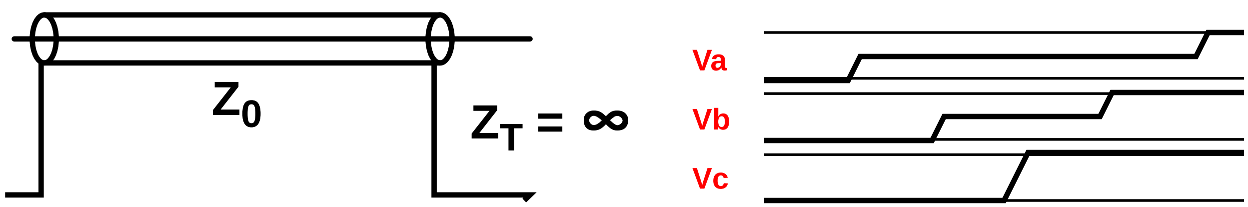
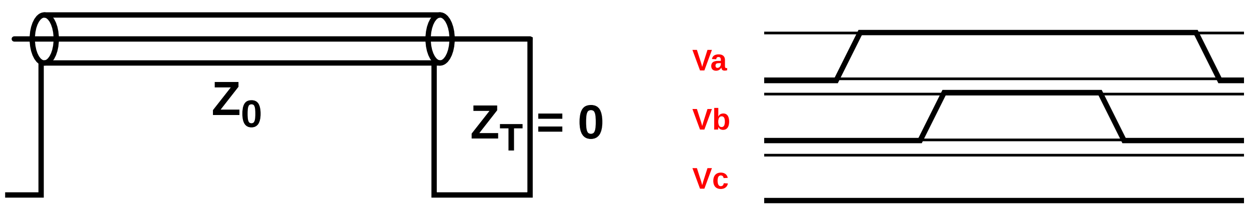
$$k_r = \frac{I_r}{I_i} = \frac{V_r}{V_i} = \frac{Z_T - Z_0}{Z_T + Z_0}$$



Matched Termination, $k_r = 0$



Open-Circuit Termination, $k_r = 1$



Short-Circuit Termination, $k_r = -1$

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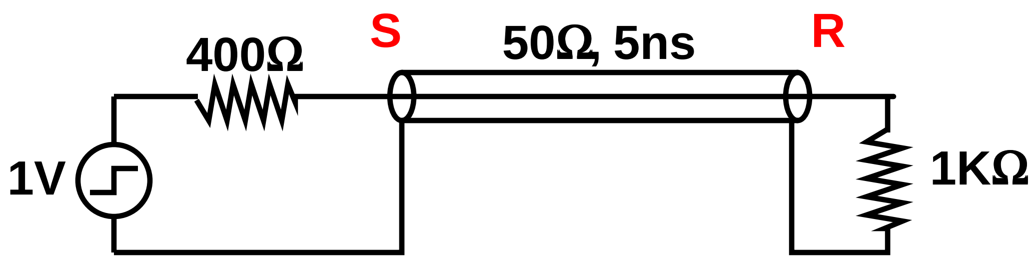

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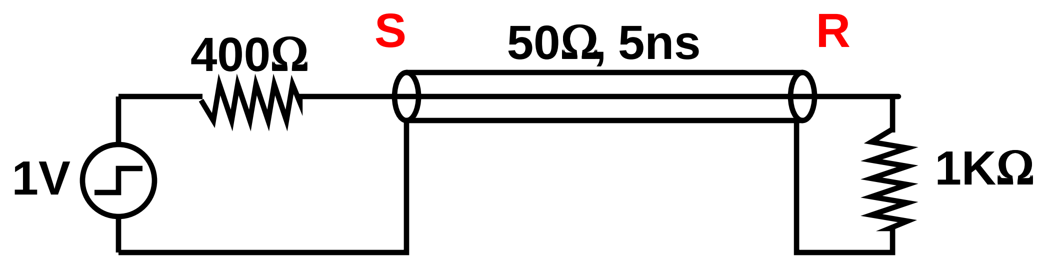

$$V_i = \left(\frac{Z_0}{Z_0 + R_S}\right)V_S = \left(\frac{50}{50+400}\right)1V = 0.111V$$

$$k_{rR} = \frac{Z_T - Z_0}{Z_T + Z_0} = \frac{1000-50}{1000+50} = 0.905$$

$$k_{rS} = \frac{Z_T - Z_0}{Z_T + Z_0} = \frac{400-50}{400+50} = 0.778$$

Values are typical for 8-mA CMOS driver with 1kΩ pullup

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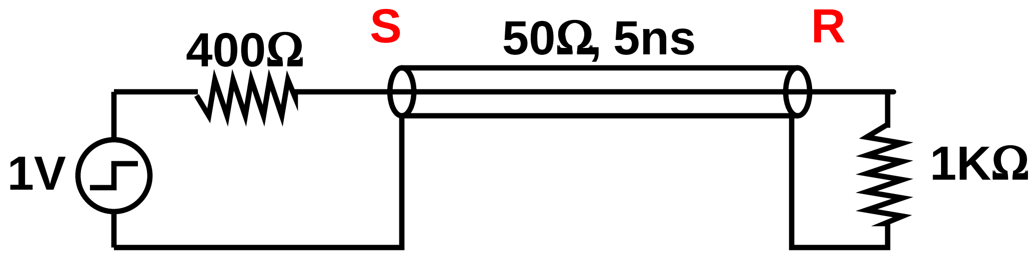
Impedance and Reflections



	Vwave	Vline	time t
Vi1	0.111	0.111	0
Vr1	0.101	0.212	5
Vi2	0.078	0.290	10
Vr2	0.071	0.361	15
Vi3	0.055	0.416	20
Vr3	0.050	0.465	25
Vi4	0.039	0.504	30
Vr4	0.035	0.539	35
Vi5	0.027	0.566	40

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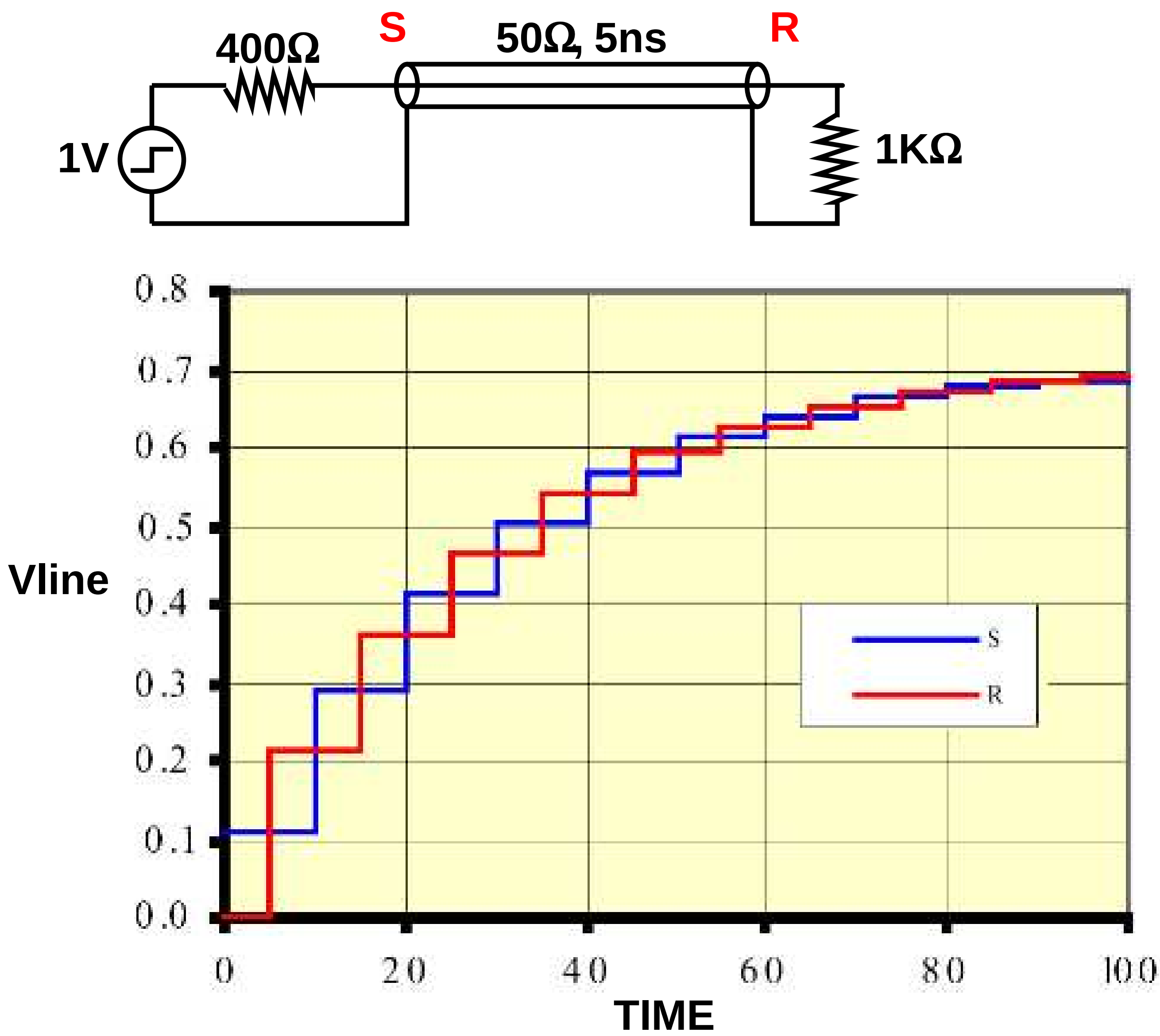

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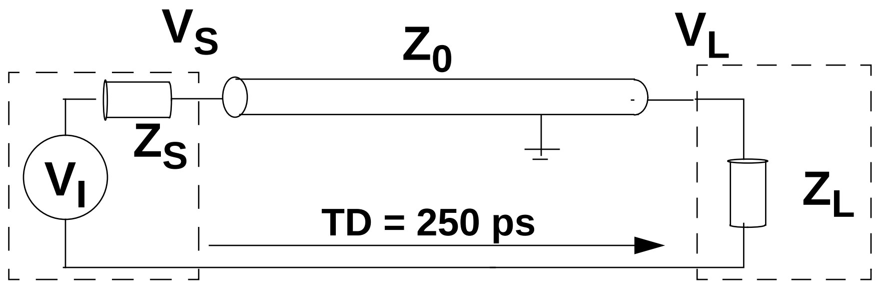
Reflections, $Z_S < Z_0$



Z_S = 25 Ω

Z_0 = 50 Ω

Z_L = inf Ω

V_I = 0v → 2v

$$V_S = V_I \frac{Z_S}{Z_S + Z_0} = 2 * \frac{50}{25 + 50} = 1.3333\text{ V}$$

$$k_{r\ (load)} = \frac{Z_L - Z_0}{Z_L + Z_0} = \frac{\text{inf} - 50}{\text{inf} + 50} = 1$$

$$k_{r\ (source)} = \frac{Z_S - Z_0}{Z_S + Z_0} = \frac{25 - 50}{25 + 50} = -0.3333$$

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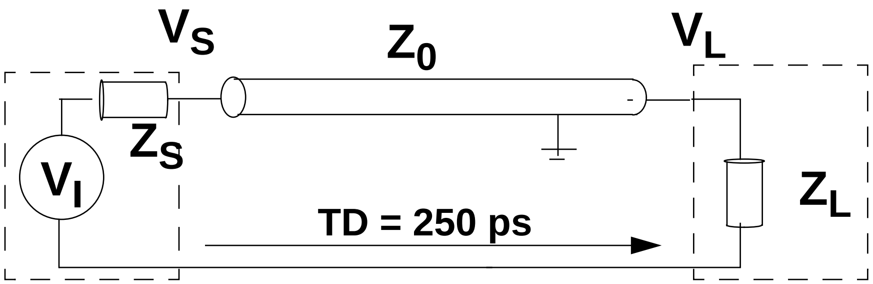
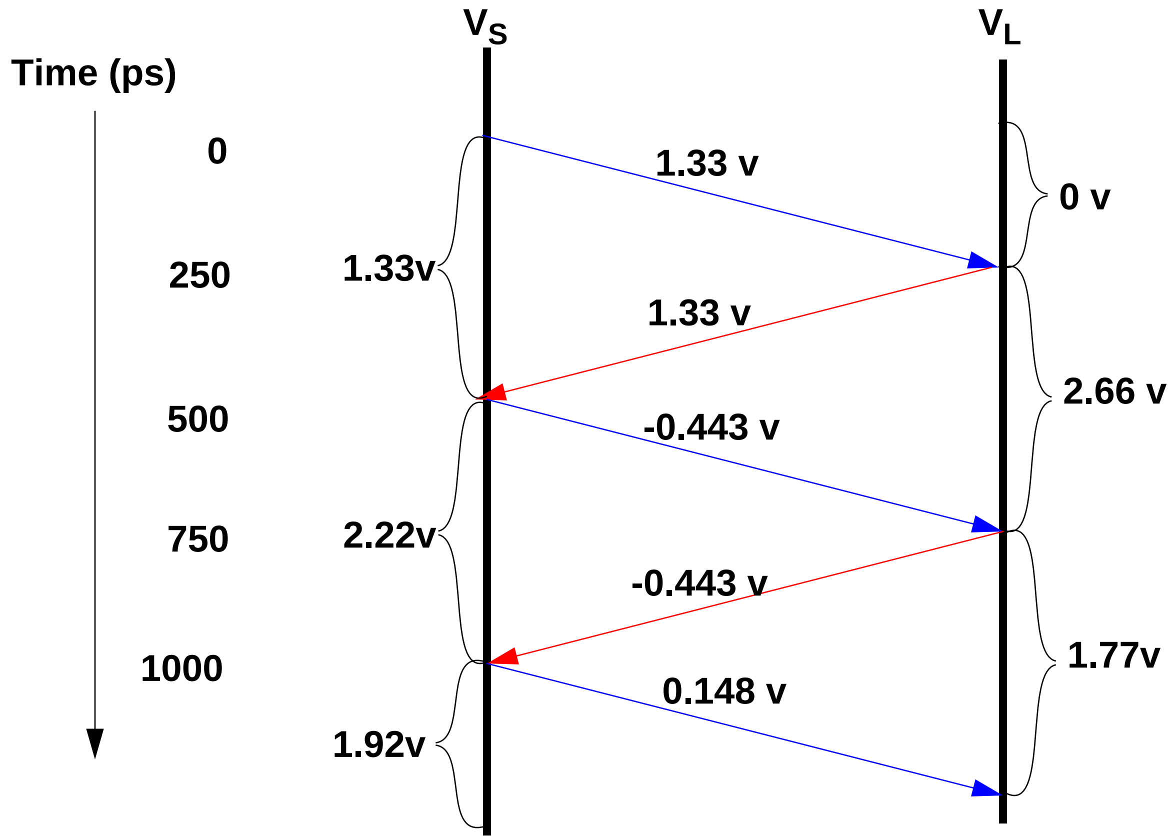
Reflections, $Z_S < Z_0$

$k_{r\ (load)} = 1$

$k_{r\ (source)} = -0.3333$





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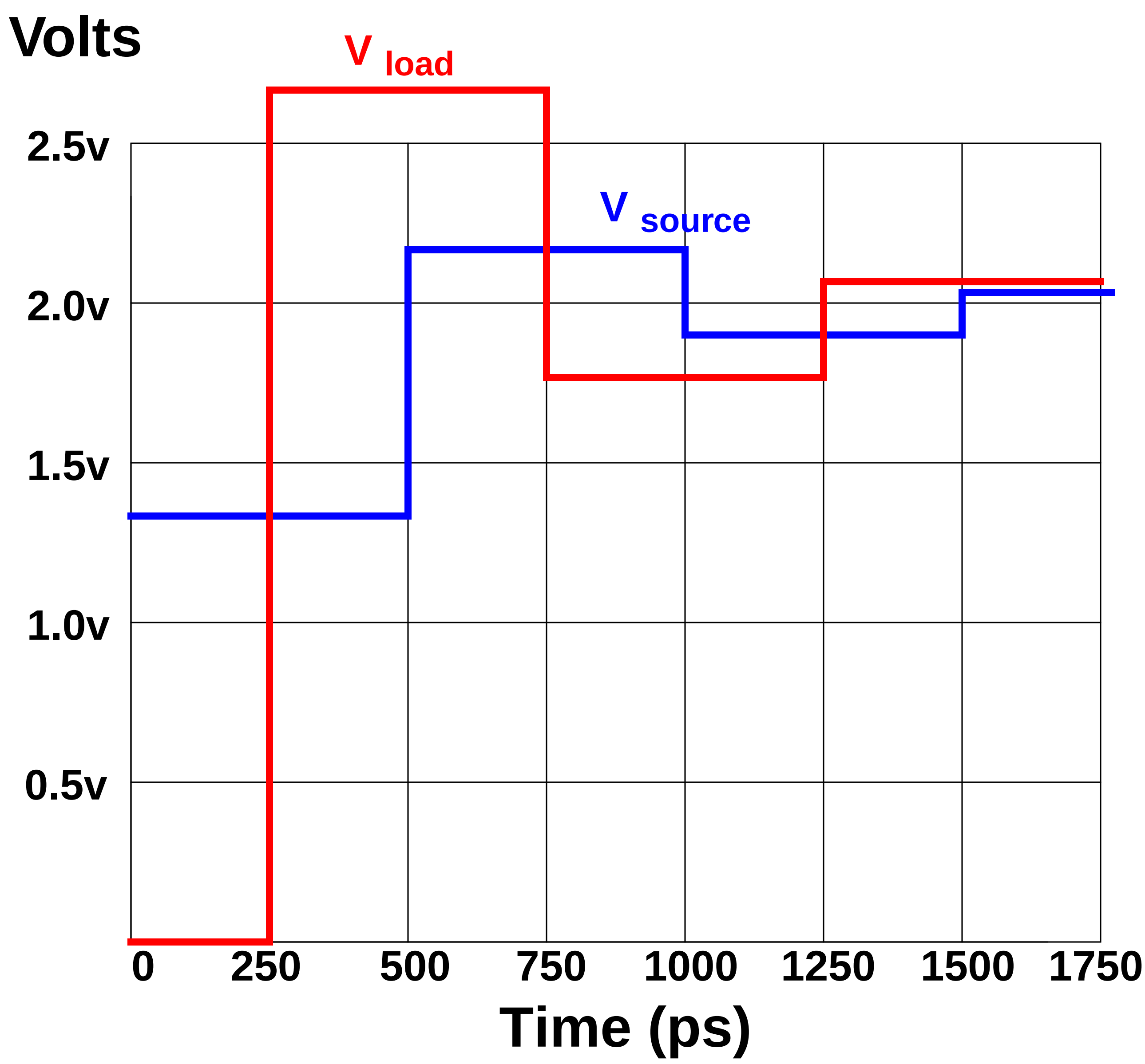
Reflections, $Z_S < Z_0$



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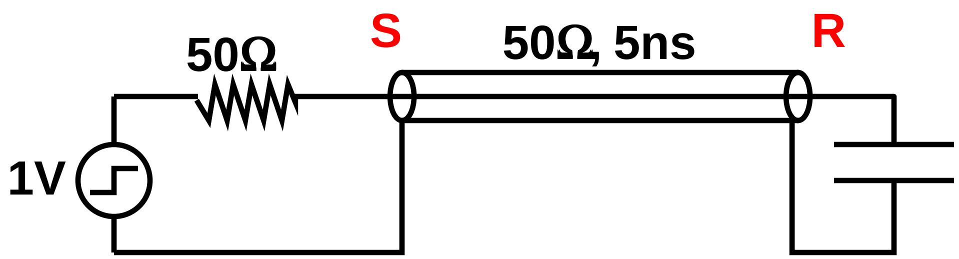
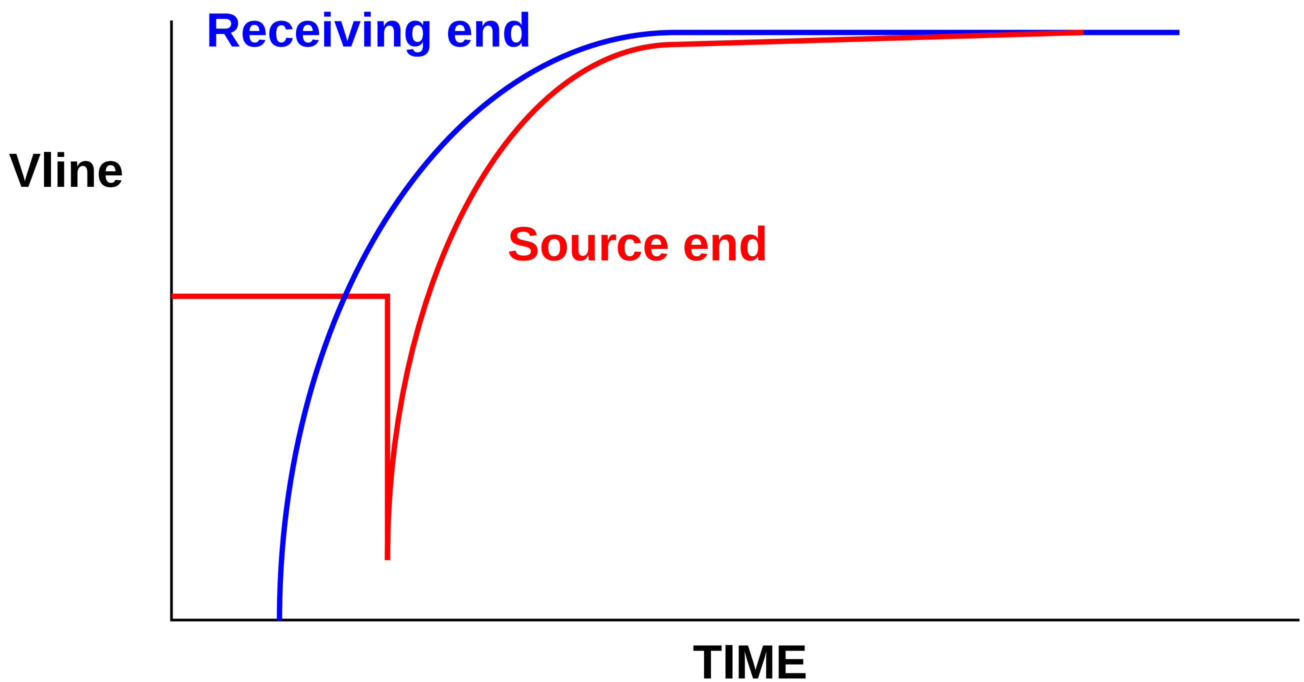
Add In Capacitance …



What if we throw in a capacitor (i.e., reality?)

Simple case: matched impedance at source end



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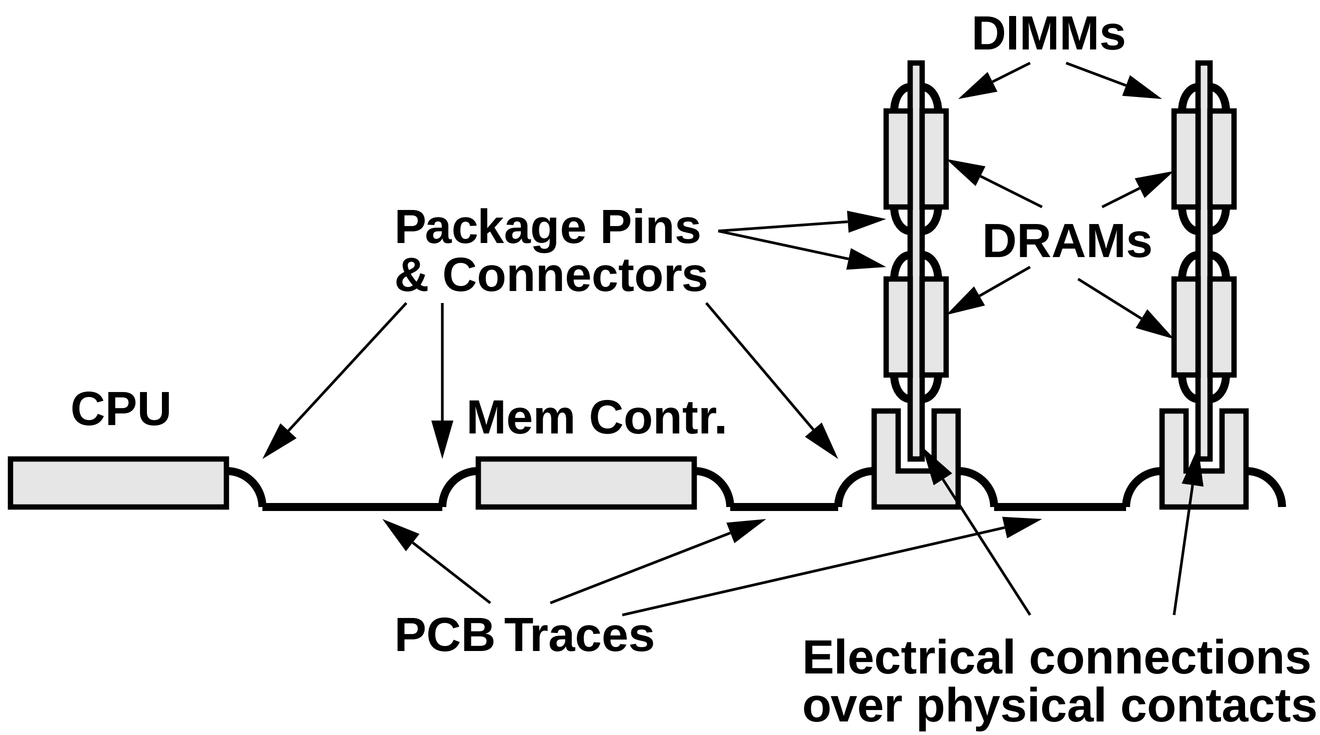
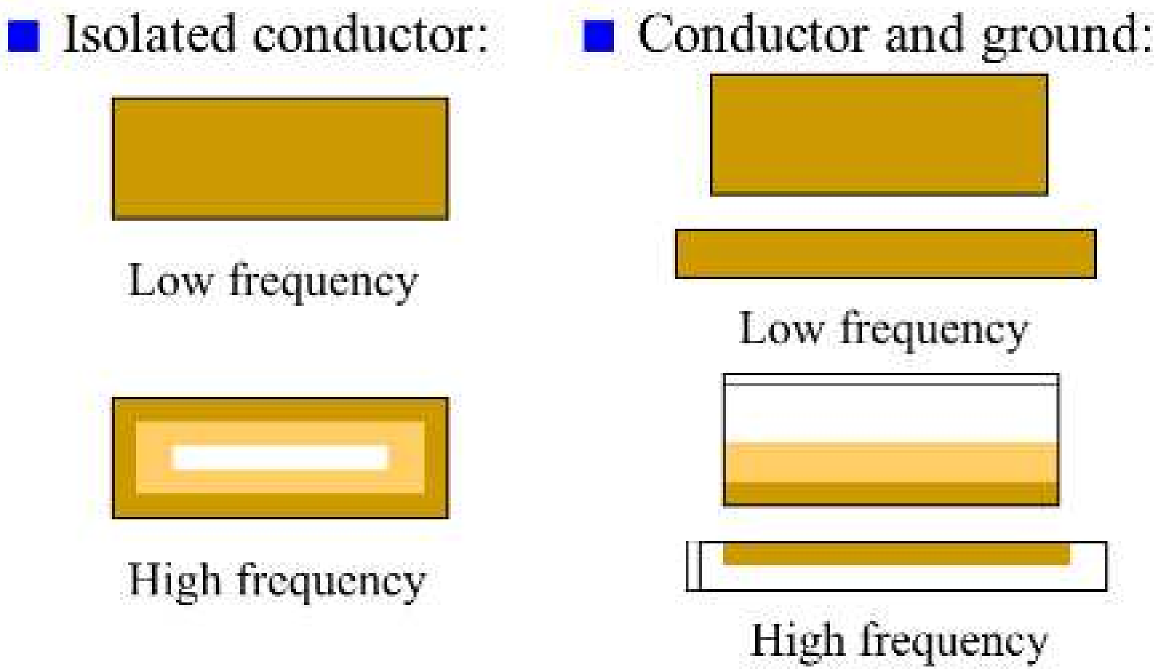
Impedance and Reflections

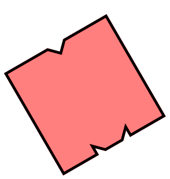


Modern systems have MANY, MANY, MANY potential sources of impedance-mismatch and/or reflections

Skin Effect

- **At low frequencies, most of conductor's cross-section carries current.**
- **As frequency increases, current moves to skin of conductor, back-EMF induces counter-current in body of conductor. Result: increased resistance, longer transmission delays.**
- **Skin effect most important at gigahertz frequencies.**





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Propagation Delay

Waves travel with velocity through medium:

$$v = (LC)^{-1/2} = (\varepsilon_{di}\,\mu_{di})^{-1/2} = c_0(\varepsilon_r\,\mu_r)^{-1/2}$$

ε is the permittivity of dielectric

μ is the permeability of dielectric

Relative permittivity ε_r and propagation speed (μ_r is typically 1 for most dielectrics):

Dielectric	ε_r	Speed (cm/ns)
Vacuum	1	30
SiO_2	3.9	15
PC Board (epoxy glass)	5.0	13
Alumina (ceramic package)	9.5	10

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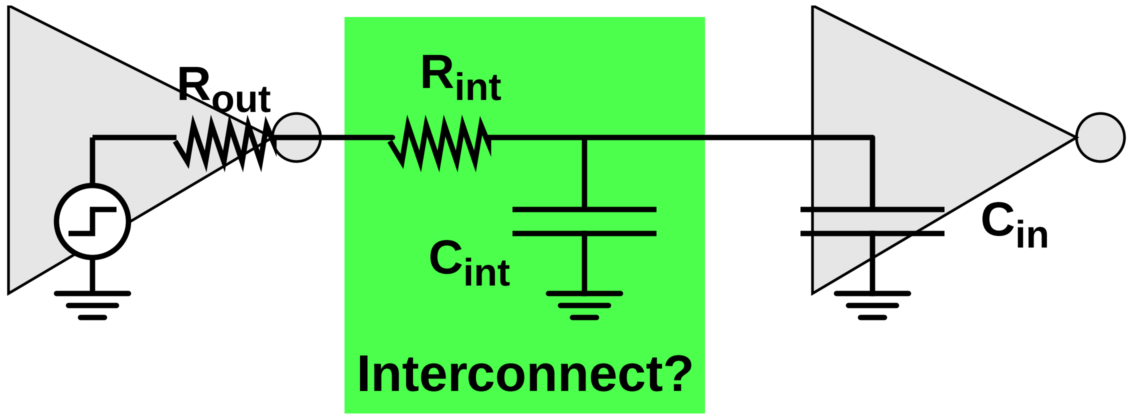
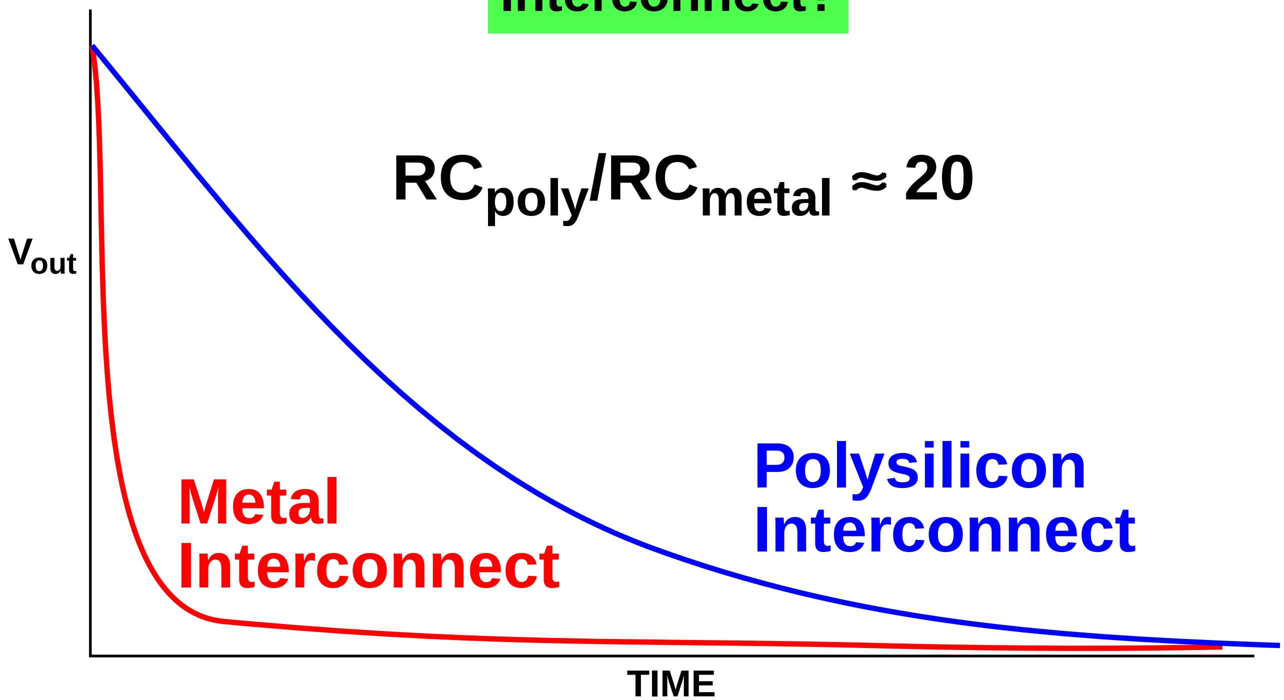
Propagation Delay

But it’s not that simple ...





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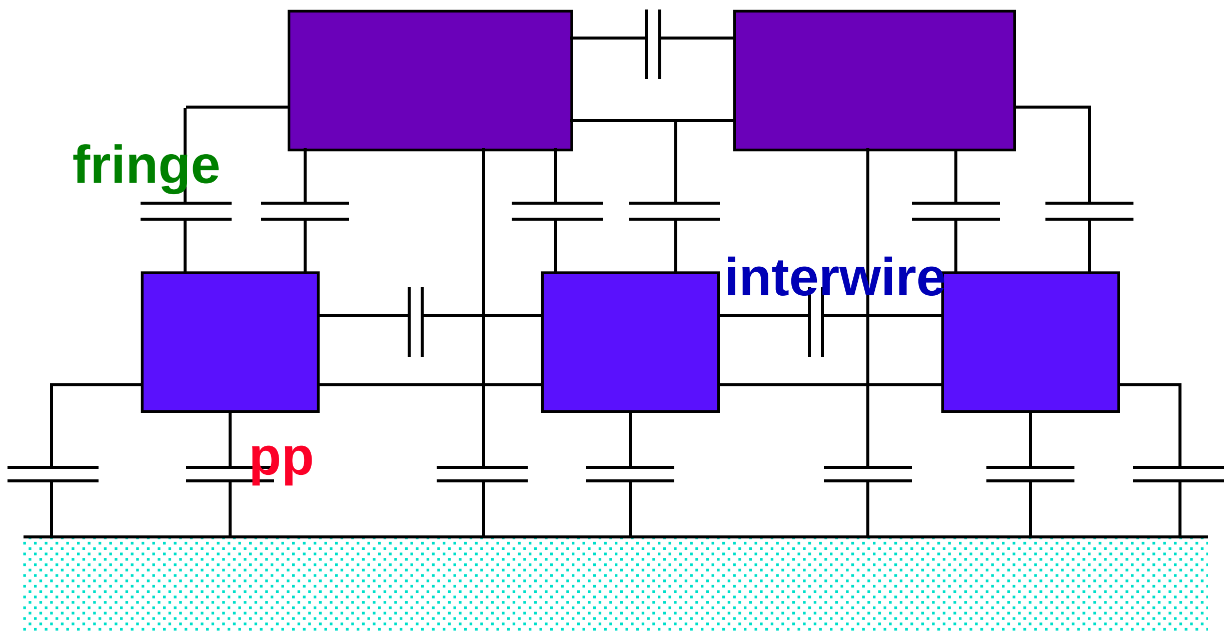
Propagation Delay

Once again, τ = RC

$$C_{wire} = C_{pp} + C_{fringe} + C_{interwire}$$
$$= (\varepsilon_{di}/t_{di})WL$$
$$+ (2\pi\varepsilon_{di})/\log(t_{di}/H)$$
$$+ (\varepsilon_{di}/t_{di})HL$$



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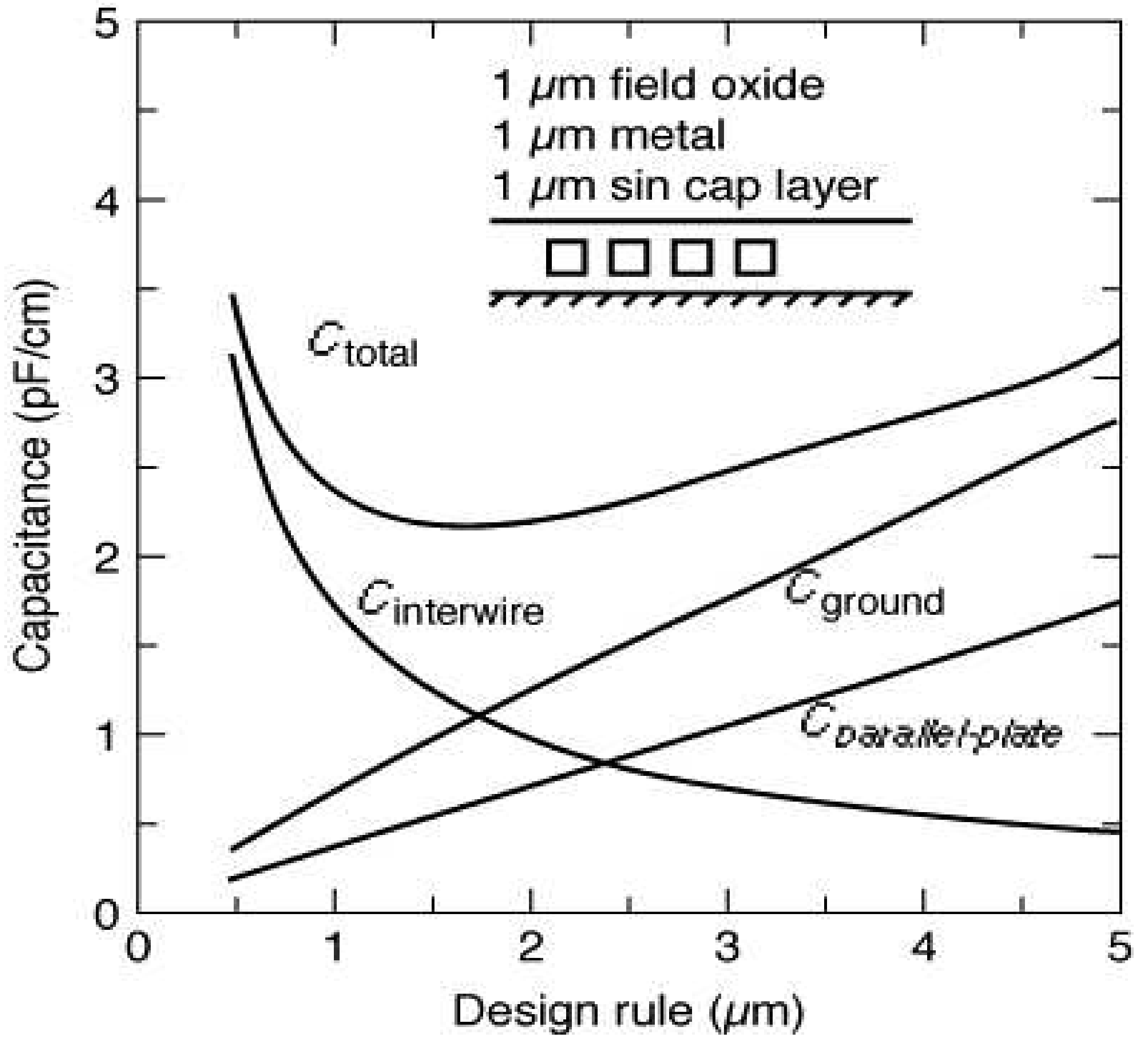
Propagation Delay



(from [Bakoglu89])

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Insights

- **For W/H < 1.5, the fringe component dominates the parallel-plate component. Fringing capacitance can increase overall capacitance by a factor of 10 or more.**
- **When W < 1.75H interwire capacitance starts to dominate**
- **Interwire capacitance is more pronounced for wires in the higher interconnect layers (further from the substrate)**
- **Wire delay nearly proportional to L^2**

Rules of thumb:

- **Never run wires in diffusion**
- **Use poly only for short runs**
- **Shorter wires – lower R and C**
- **Thinner wires – lower C but higher R**

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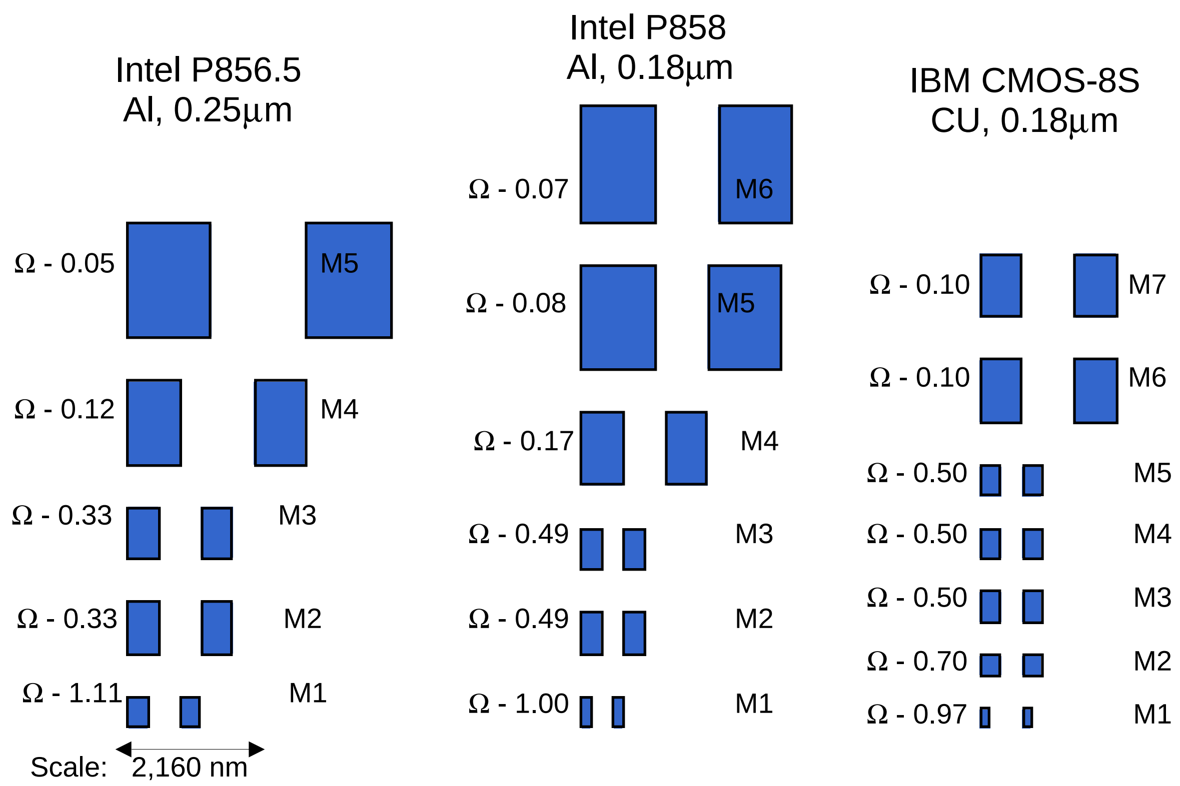
Wire Spacing



from MPR 2000

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Overcoming Interconnect R

Selective technology scaling
(scale W while holding H constant)

Use better interconnect materials

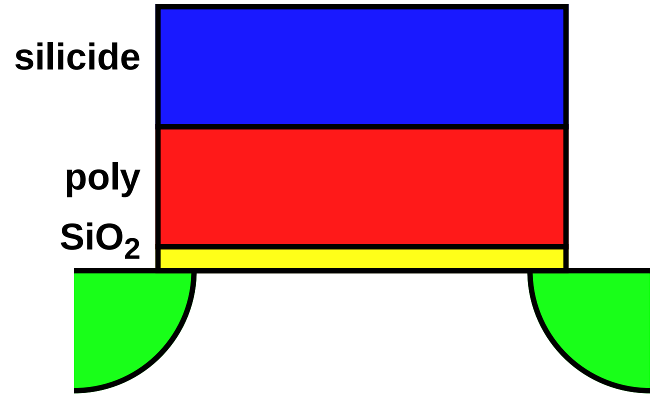
- **lower resistivity materials like copper**

As processes shrink, wires get shorter (reducing C) but they get closer together (increasing C) and narrower (increasing R). So RC wire delay increases and capacitive coupling gets worse.

Copper has about 40% lower resistivity than aluminum, so copper wires can be thinner (reducing C) without increasing R

- **use silicides (WSi2, TiSi2, PtSi2 and TaSi)**

Conductivity is 8-10 times better than poly alone



Use more interconnect layers

reduces the average wire length L, but beware of extra contacts

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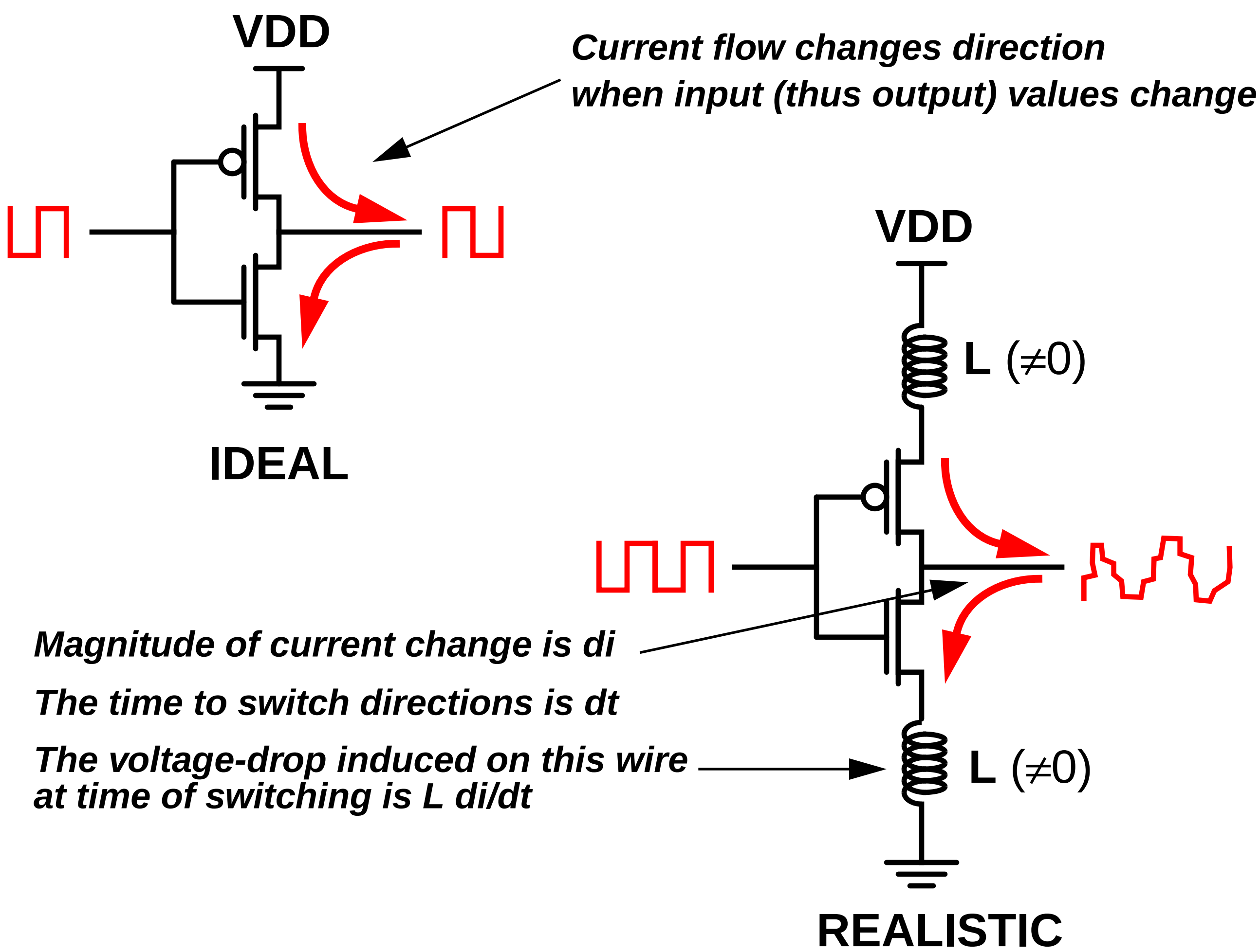
Inductive Noise

L di/dt noise (ground bounce):



Current flow changes direction when input (thus output) values change

Magnitude of current change is di

The time to switch directions is dt

The voltage-drop induced on this wire at time of switching is L di/dt

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Inductive Noise

L di/dt noise (ground bounce):