ENEE 359V, Advanced Digital Design with Hardware Description Languages, 2-credits

Text books:
Required: Advanced Digital Design With the Verilog Hdl, *by M. Ciletti, Prentice Hall, 2003.*
Recommended: Verilog Styles for Synthesis of Digital Systems, *by D. Smith and P. Franzon*

Meetings:
- One 75' lecture
- 2 hours lab led by the Instructor

Topics:
1. Review of Combinational and Sequential Digital Logic Design
2. Basic Verilog Language Structures (Datatypes, Modules, etc.)
   - Datatypes: nets, registers, event, bitvectors, arrays, parameters
   - Modules: ports, hierarchical names
3. Structural and Behavioral Specifications
   - Basic gates, User-defined primitives, Modeling levels
   - Synthesizable operations, Continuous assignments (Examples: *Adders*, *ALU*)
4. Simulation. Testbenches and debugging.
5. Synthesis flow. Synthesis to Standard cells and FPGA.
6. Procedural Specifications and Designing Single Modules
   - The *always* block
   - Functions and Tasks
   - Blocking and Non-blocking assignments
   - Control constructs and their Synthesis
   - Design examples: *Counters*, *Unsigned Multiplier*
   - Validation: Verification Vectors, Testbench Coding Approaches, Post-synthesis verification
7. Finite State Machine Specifications and Styles
   - Explicit and Implicit Specification Styles
   - Example: *Booth multiplier*
   - Example: *First-in-First-Out buffer (FIFO)*
8. Design Reuse
   - Instantiation of parametrized modules.
   - Control-point style for design reuse (Examples with *FIFO*)
   - Using vendor components (*Booth multiplier*)
9. Improving Timing, Area, and Power
   - Delay calculations
   - Timing design with Flip-flops and Latches
   - Low-power design issues and Area considerations.

Students use FPGA boards for 2 (two) project assignments during the semester. A final project will be required that involves the design, implementation, and evaluation of a complex digital system. Digilent, Spartan3 (Nexys2) FPGA boards will be used. Complete CAD software (simulation and synthesis) freely available from Xilinx – ISE WebPack.

Grading:
Two (2) project assignments: 15% each
Final project (written report and a demonstration): 35%
Final exam: 30%
Lab and class participation: 5%