Design a fabrication process for the Metal Oxide Semiconductor (MOS) capacitor shown in the figure. Assume that the via width is the critical dimension (the electrode dimensions are much larger) and that the substrate is highly doped (no additional doping is necessary to make contact). The oxide thickness is 0.1 µm. Perform the design for two different cases of via width: 10 µm and 0.1 µm. In each case, choose the most cost-effective lithography and etching methods that can still provide the desired result and explain your choice.

List in detail all the steps for fabricating the device starting with a blank substrate. For each fabrication step, draw a cross section view of the device. In addition, for each lithography step draw an outline of the mask, indicate the mask polarity, and specify the type of photoresist (positive or negative).

Note: Since oxide deposition methods have not been covered yet in class, you do not need to specify how it is deposited, and may just list it as "deposition".