# Damascene Process and Chemical Mechanical Planarization

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# Background

- Traditionally, IC interconnects formed from Aluminum
- Interconnects produced by subtractive etching of blanket Aluminum, defined by the photoresist pattern
- Over the past two decades, IC scaling and performance needs necessitated the change in metal from Aluminum to Copper

# Transition from Aluminum to Copper

- The primary motivation behind the transition is increased demand in:

  I. Performance
    - Copper has lower resistivity than Aluminum
    - Lower resistivity leads to higher performance

  II. Scaling
    - Lower resistivity leads to lower Joule Heating
    - Allowing higher current densities and therefore smaller sizes

  III. Reliability
    - Copper has lower activation energy than Aluminum
    - Copper is more resistive to Electromigration failures than Aluminum
    - Copper has higher thermal conductivity, providing efficient heat conduction paths

# Challenges with Copper

I. Difficult to pattern using conventional etching techniques
   - Copper does not produce a volatile by-product during etching
   - For example, Chlorine gas (used to etch metals in plasma etchers) forms chloride that will not readily evaporate

II. Junction spiking/Copper Poisoning
   - Quickly diffuses into oxides and silicon
   - Spikes could be long enough to penetrate through junction

III. Poor oxidation/corrosion resistance
   - Quickly oxidizes in air and does not protect the underlying copper from further oxidation

# Solution

- In 1990s, IBM introduces Damascene Process
- A means for forming copper IC interconnects
- Damascene Process – a unique additive processing technique
- Reminiscent of the metal inlay techniques used in the Middle East since the middle ages.
- The name originates in Damascus, the capital of modern Syria

# Damascene Process

- Addresses the challenges copper presents by:
  - Eliminating the need to etch copper
    - Uses Chemical Mechanical Planarization (CMP) instead of etching
  - Using special barrier layers to stop copper diffusion
    - Barrier layers prevent the intermixing of materials above and below the barrier
    - Typical barrier materials are Ta, TaN, TiN, and TiW

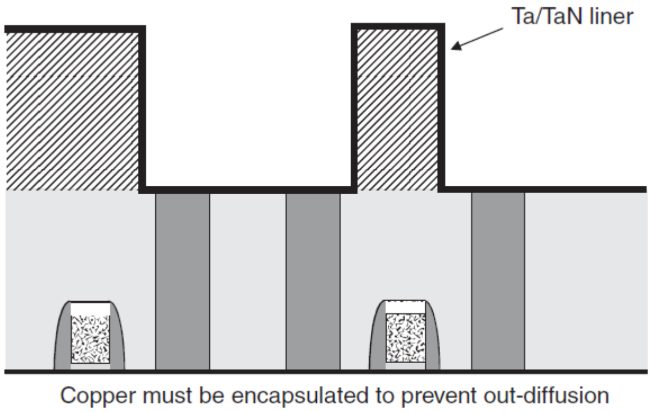
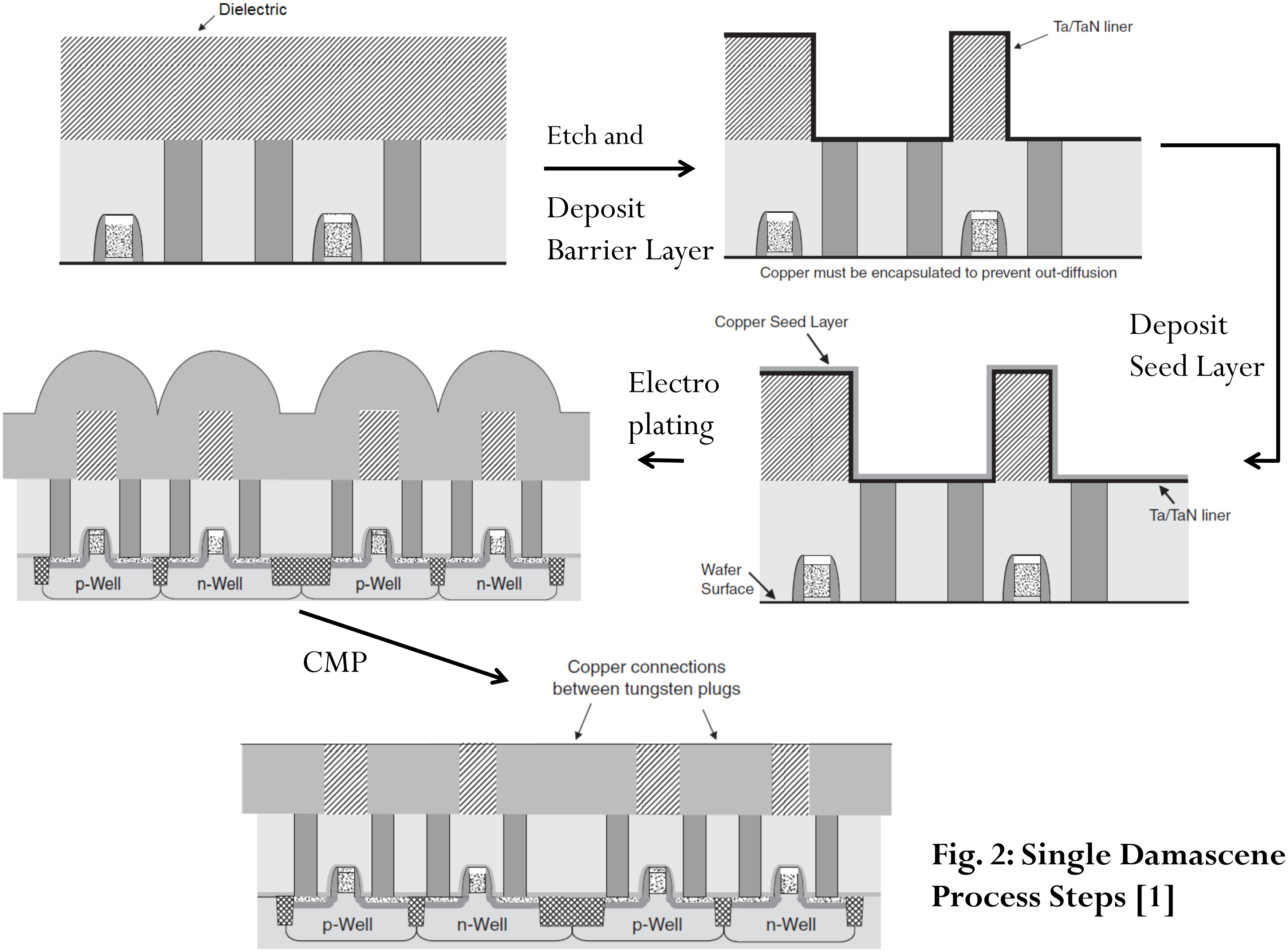


**Fig. 1: Barrier Layer [1]**

# Damascene Process Steps

- Damascene is an additive process
- Firstly, the dielectric is deposited
- Secondly, the dielectric is etched according to the defined photoresist pattern, and then barrier layer is deposited
- Thirdly, copper is deposited
- Optimum way of copper deposition is electroplating
- Copper electrodeposition is a two step process
  - First seed layer is deposited on the wafer using PVD
  - Next the copper is electroplated
- Finally, the surface is planarized using CMP



Etch and

Deposit
Barrier Layer

Deposit
Seed Layer

Electro
plating

CMP

**Fig. 2: Single Damascene Process Steps [1]**

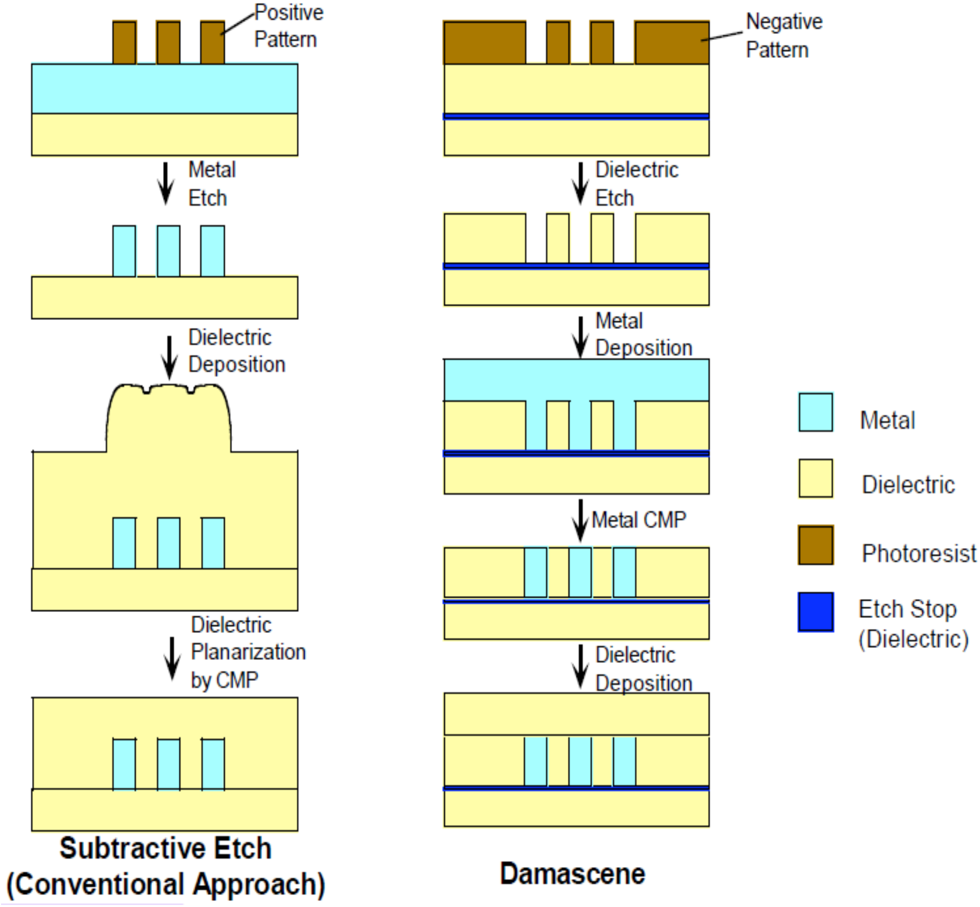
# Conventional Metallization Process versus Damascene Process

Depositing **metal** and defining PR pattern

Metal is etched according to PR pattern

Dielectric is deposited

Excess dielectric is etched



Depositing **dielectric** and defining PR pattern

Trenches for vias and lines are etched

Metal fills the trenches

Excess metal is removed by CMP

Dielectric is re-deposited

**Fig. 3 : Comparison of conventional metallization process with Damascene Process [2]**

# Dual Damascene Process

- Very similar to single damascene process, key difference is "dual"
- Creates vias and lines by etching holes and trenches in the dielectric, and then depositing copper in both features
- One photo/etch step to make holes (vias) in the dielectric so as to make connection with underlying metal
- Second photo/etch step to make trenches for the metal line
- The two photo/etch steps can be performed in two orders:
    i. Trench First then Via
    ii. Via First then Trench

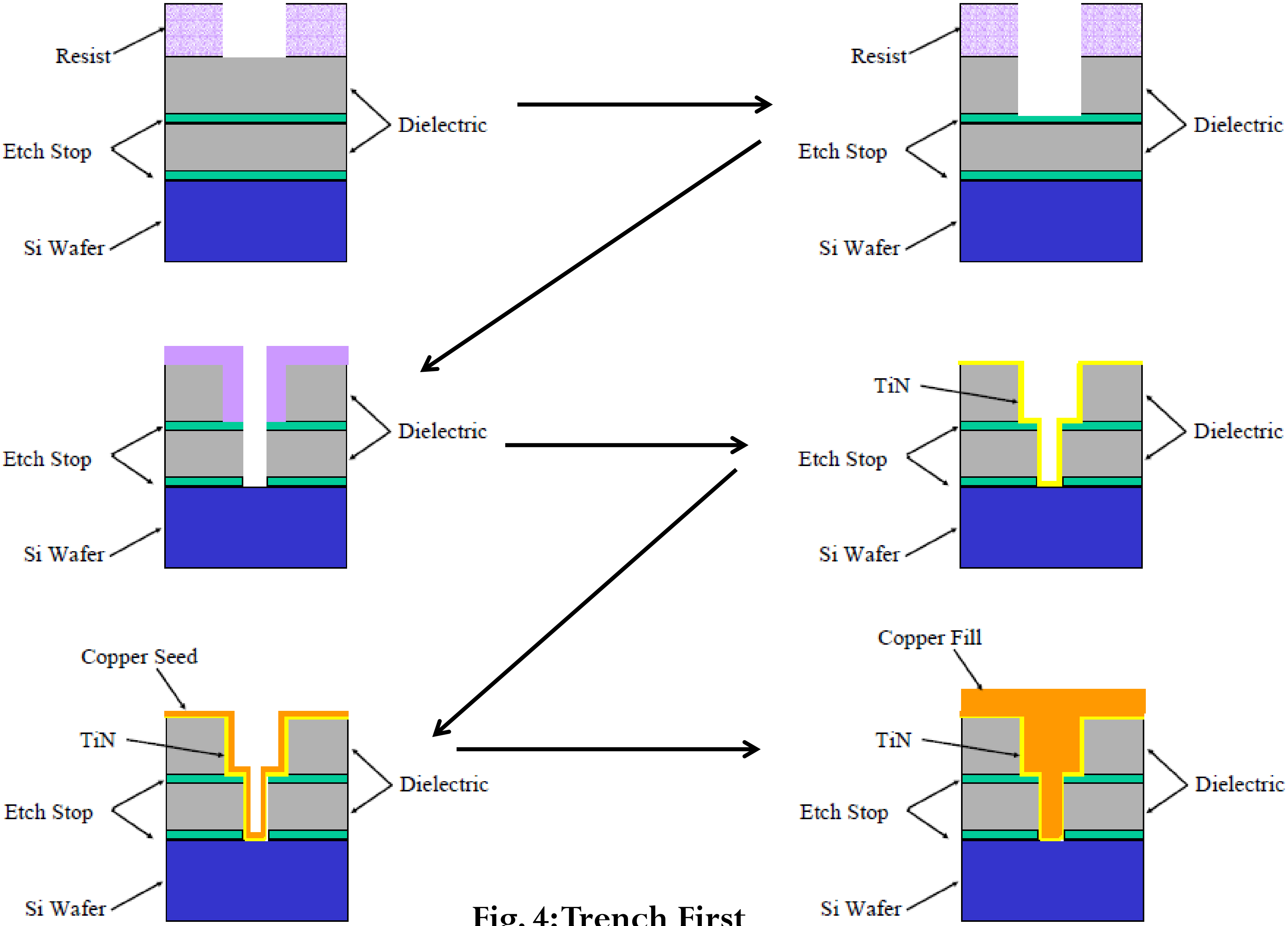


**Fig. 4:Trench First then Trench [4]**

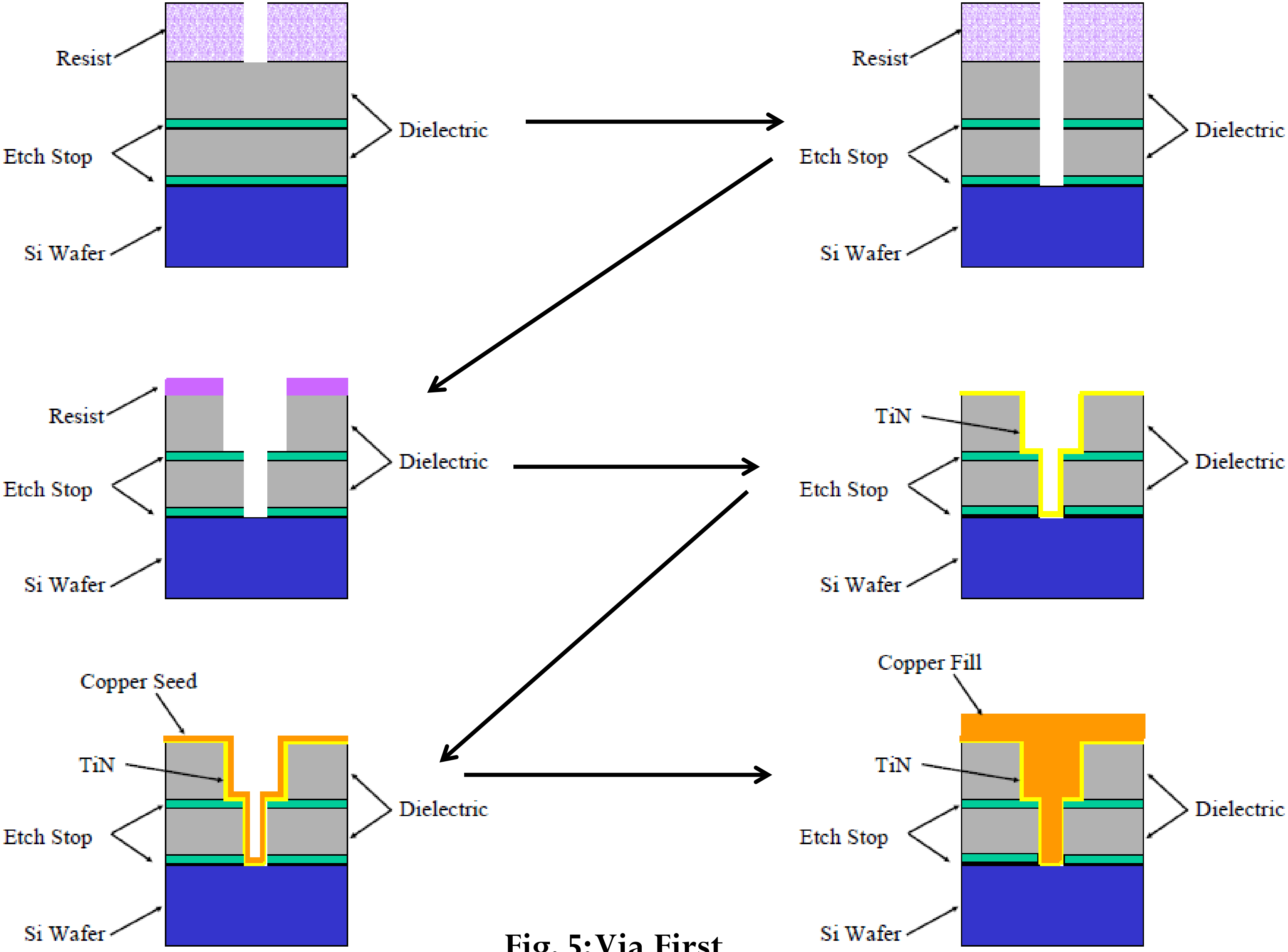


**Fig. 5: Via First then Trench [4]**

# Challenges with Dual Damascene Process

- Via first then Trench approach
  - Residual photoresist remains in the bottom of the via during the trench etch
    - Due to highly porous nature of low-K dielectrics, the residual photoresist is absorbed, thereby altering the K value of dielectric
- Trench first then Via approach
  - Photoresist also pools in the open trench structure prior to via patterning
- Most low-K dielectric films are hydrophilic
  - It is critical that surface hard mask (Photoresist) shield the dielectric from moisture as well as protect dielectric from aggressive cleans

# Chemical Mechanical Polishing/Planarization

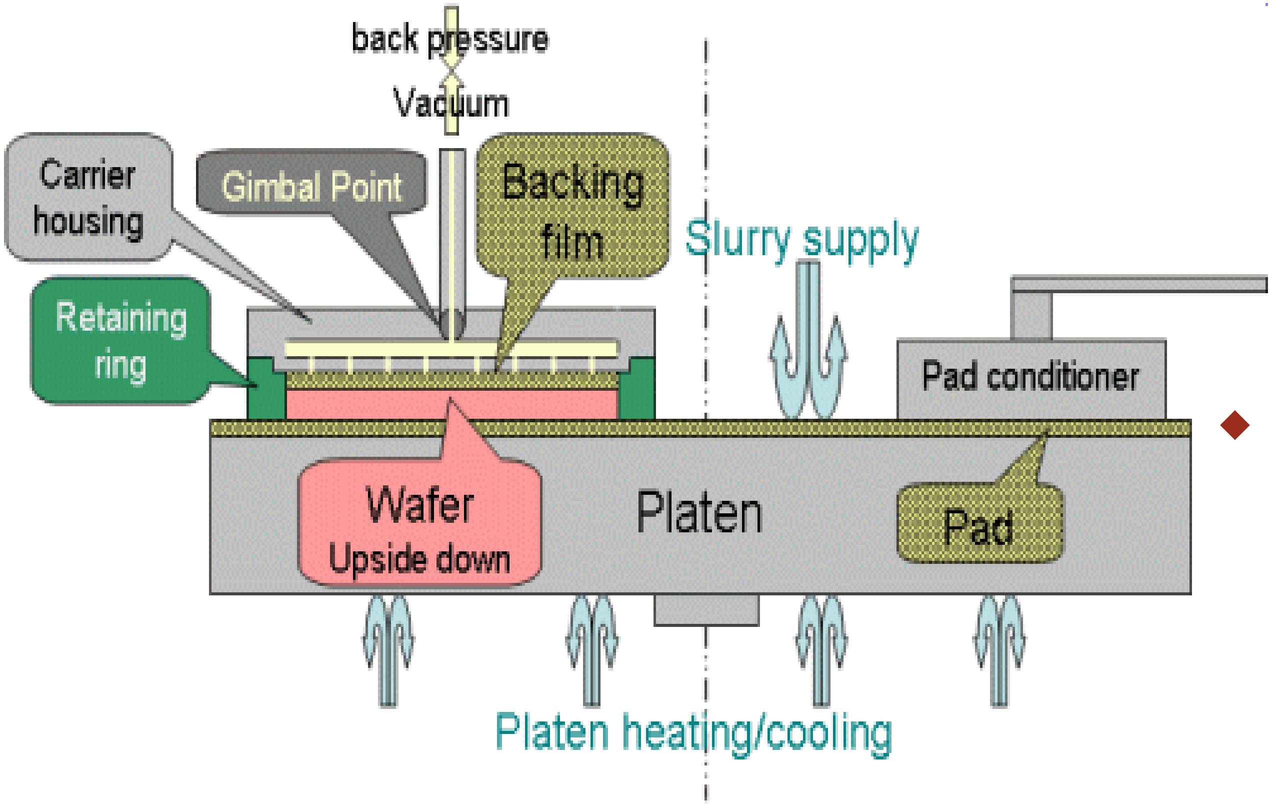


Figure 6. Basic design of CMP [5].

- **CMP** is a process of smoothing surfaces with the combination of chemical and mechanical forces.

- Typical Process Conditions
  - Pressure: 2 to 7 psi
  - Temperature: 10 C to 70 C
  - Platen/Carrier rpm: 20 to 80
  - Slurry flow rate: 100 to 200 mL/min
  - Typical removal rates:
    - Oxide CMP ~2800Å/min
    - Metal CMP ~3500Å/min

# How CMP works

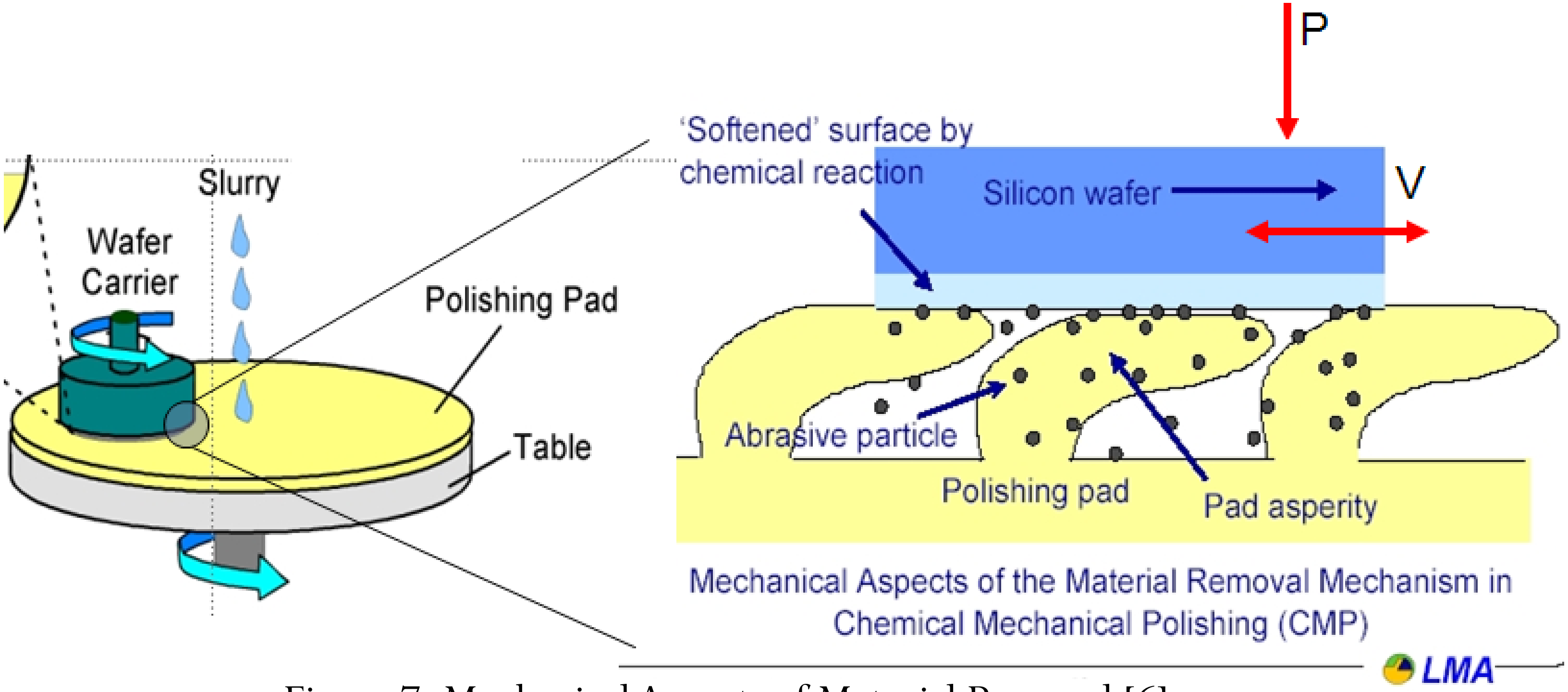


Figure 7. Mechanical Aspects of Material Removal [6].

$$\frac{dz}{dt} = -K_p \cdot \left(P \cdot V\right)$$

**[Preston's Equation, 1927]**

$\frac{dz}{dt}$ **: Material Removal Rate**

$K_p$ **: Preston Coefficient**

P = Pressure
V = Velocity

# Advantages of CMP

- Good selectivity (No lapping)
- Reduce resist thickness variation
- Better resolution of photolithographic process by reducing depth of focus
- Multi-level structures
- Improved step coverage of subsequent layer deposition

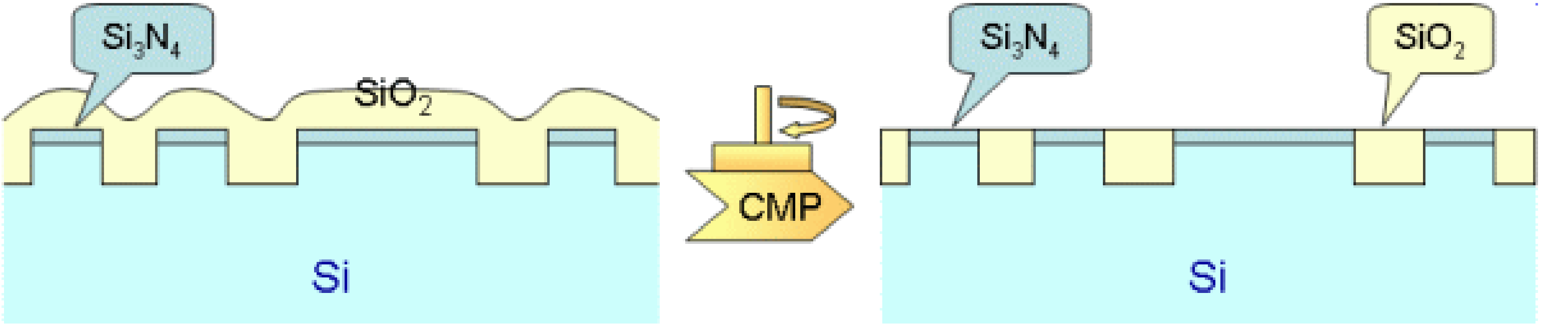


Figure 8. Oxide Planarization [5].

# Advantages of CMP cont.

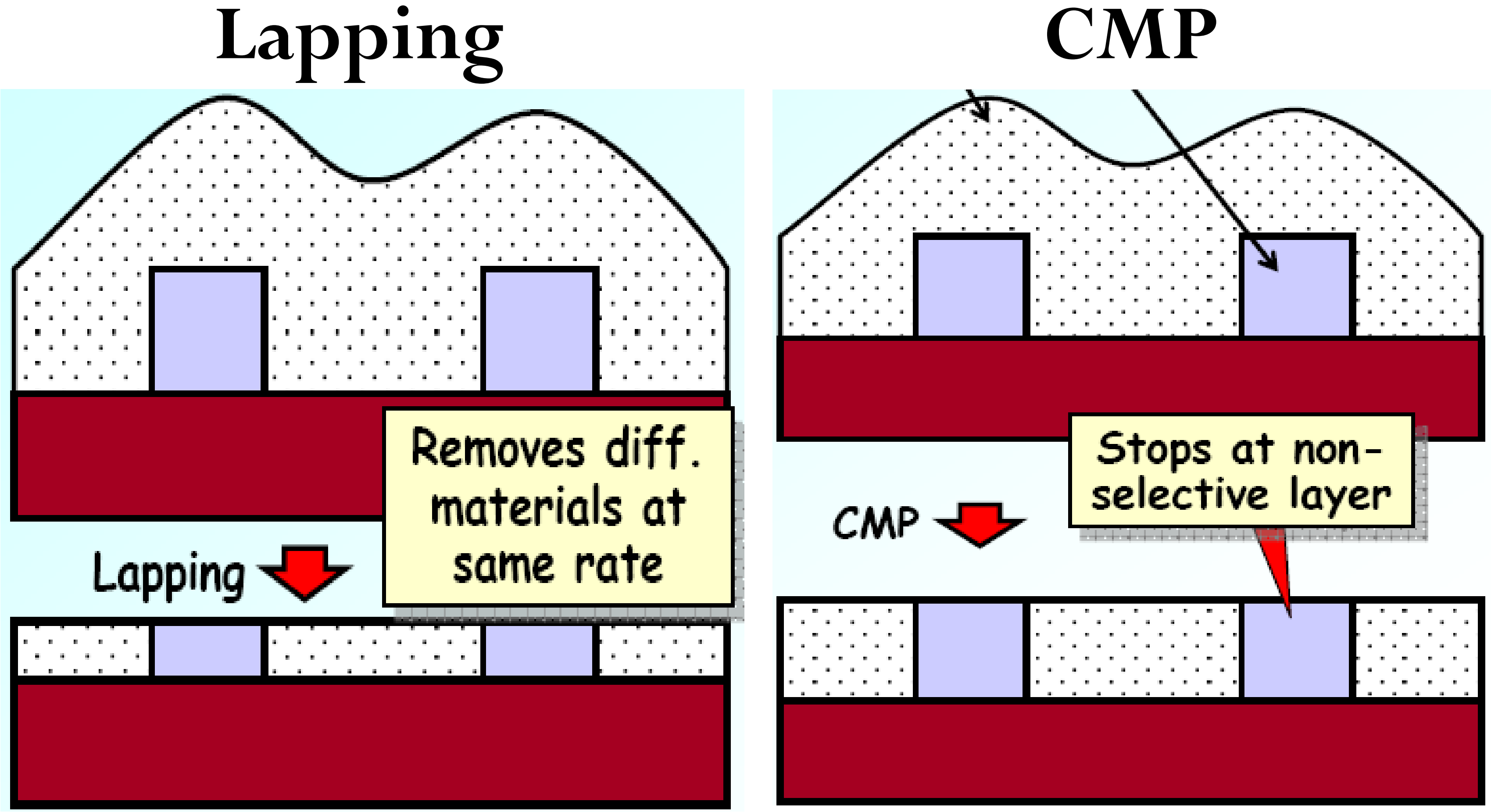


Figure 9. Better selectivity of CMP [6].

# Advantages of CMP cont.

Lithography: Resolution

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Depth of Focus

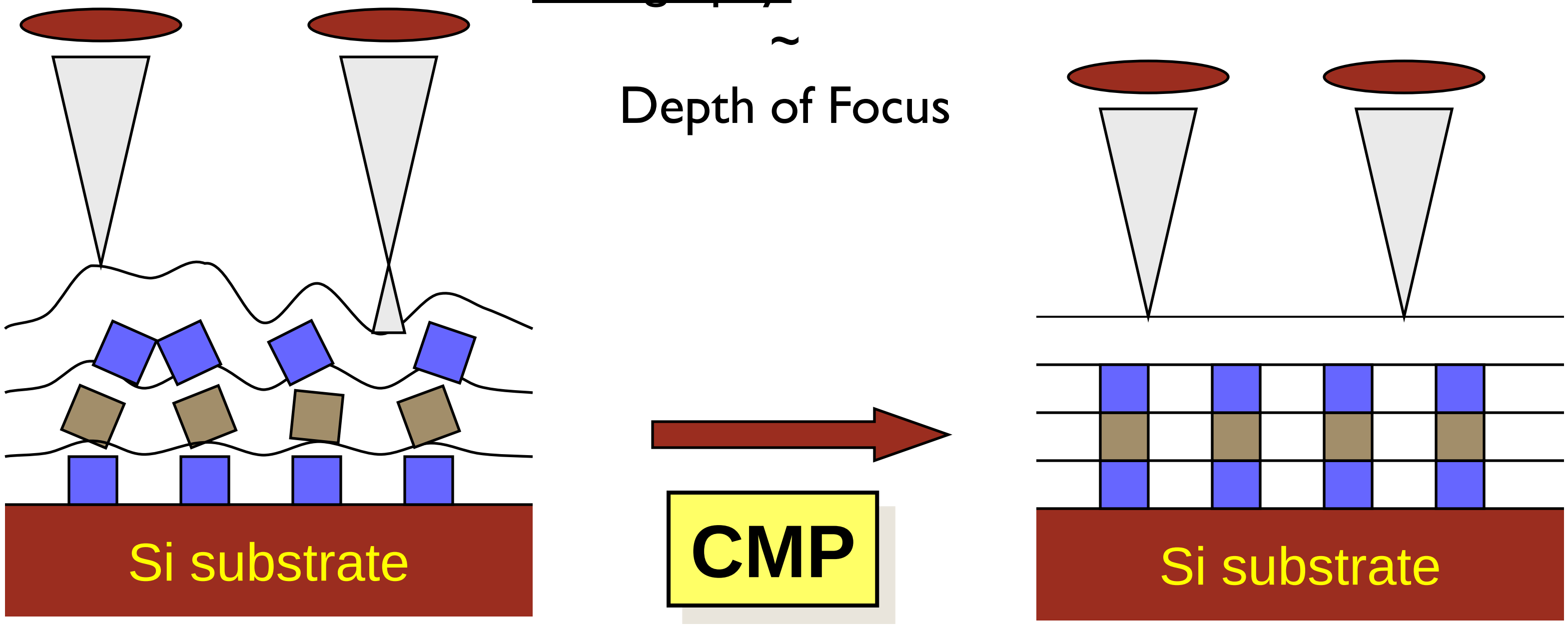

Figure 10. Effect of CMP on photolithography resolution [6].

# Types of Planarization

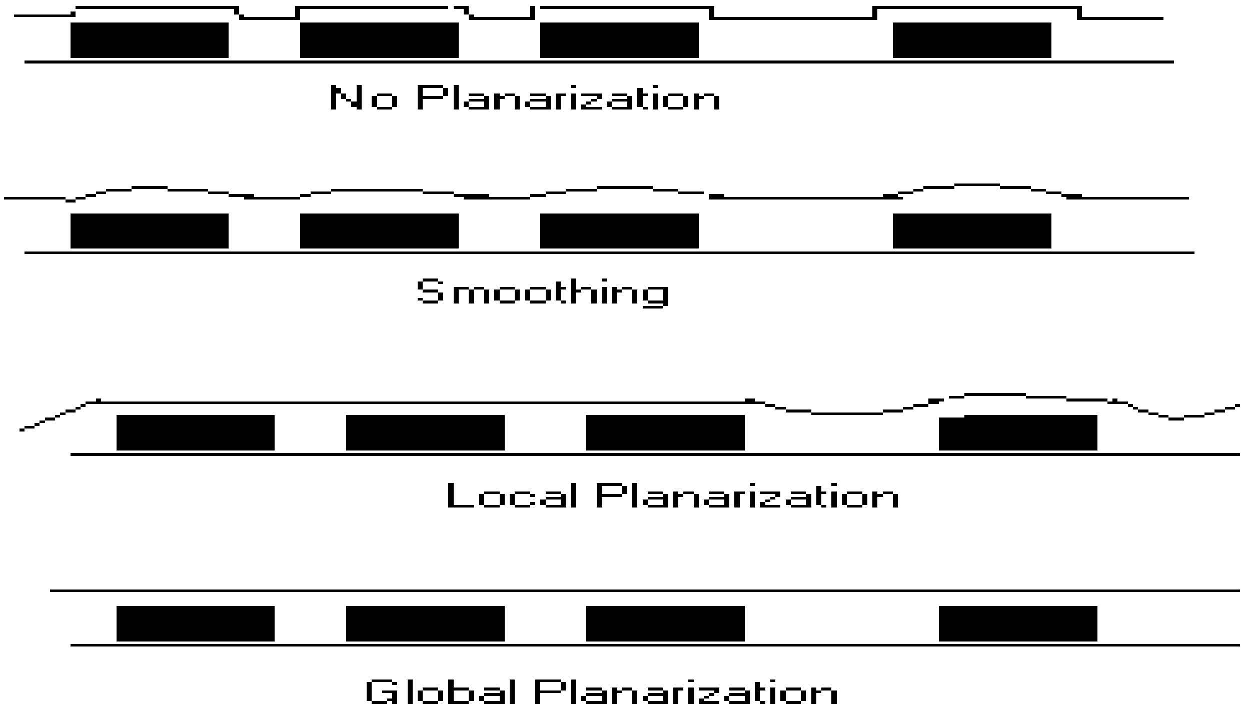

Figure 11. Various forms of planarization [7].

# Limitations of CMP

- Dishing and erosion
- Stress cracking
- Scratching
- Corrosive attacks from slurry chemicals
- Time-consuming
- Expensive

# Limitations of CMP cont.

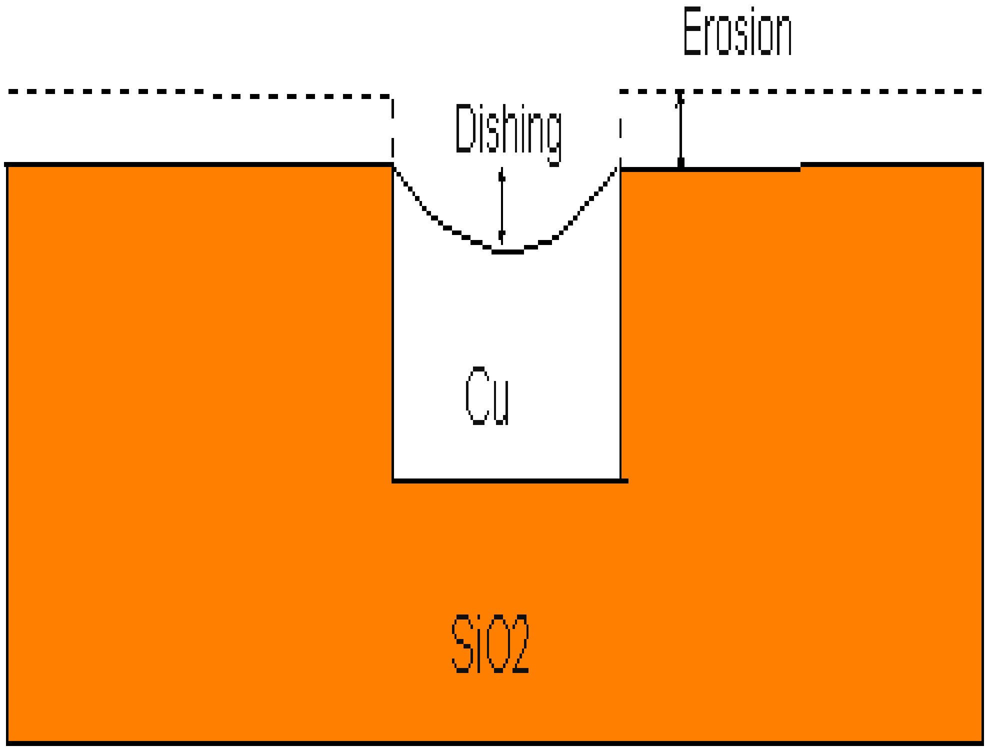

Figure 12. Illustration of copper dishing and oxide erosion [7].

- Dishing and erosion are forms of local planarization where some areas of wafer polish faster than the other.

- Multi-million $ machine (Nikon)
- Dry in Dry out
- 4 polishing tables
- Max. potential throughput of ~2,000 wafers/day

Figure 13. Nikon CMP machine [6].

Figure 14. E550 Alpsitec Company machine [5].

# Questions

# References

[1] Richard et al., "*Demystifying Chipmaking*", Elsevier, 2005.

[2] Robert Doering and Yoshio Nishi, Eds., "*Handbook of Semiconductor Manufacturing Technology*", 2nd ed., CRC Press, 2007.

[3] Michael Quirk and Julian Serda, "*Semiconductor Manufacturing Technology*", 1st ed., Prentice Hall, 2000.

[4] San Jose University Engineering Department, "*Copper Deposition*", [Online], Available: http://www.engr.sjsu.edu/sgleixner/mate166/LectureNotes/Copper%20and%20Damascene_S.pdf [Accessed: 17 Oct. 2011]

# References

[5] Alpsitec SARL. "*Alpsitec is represented by Crystec Technology Trading GmbH*," http://www.crystec.com/alpovere.htm.

[6] Joshua Chien, University of California Berkeley, CA, *Chemical Mechanical Planarization*. [Microsoft PowerPoint]. Berkeley, CA: Rohm & Haas.

[7] Jeffrey Rockwell and Yuzhuo Li, "Chemical Mechanical Polishing," 2000, http://www.files.chem.vt.edu/confchem/2000/a/rockwell/rockwell.htm.