Aligned Wafer Level Bonding

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What is Aligned Wafer Level Bonding?

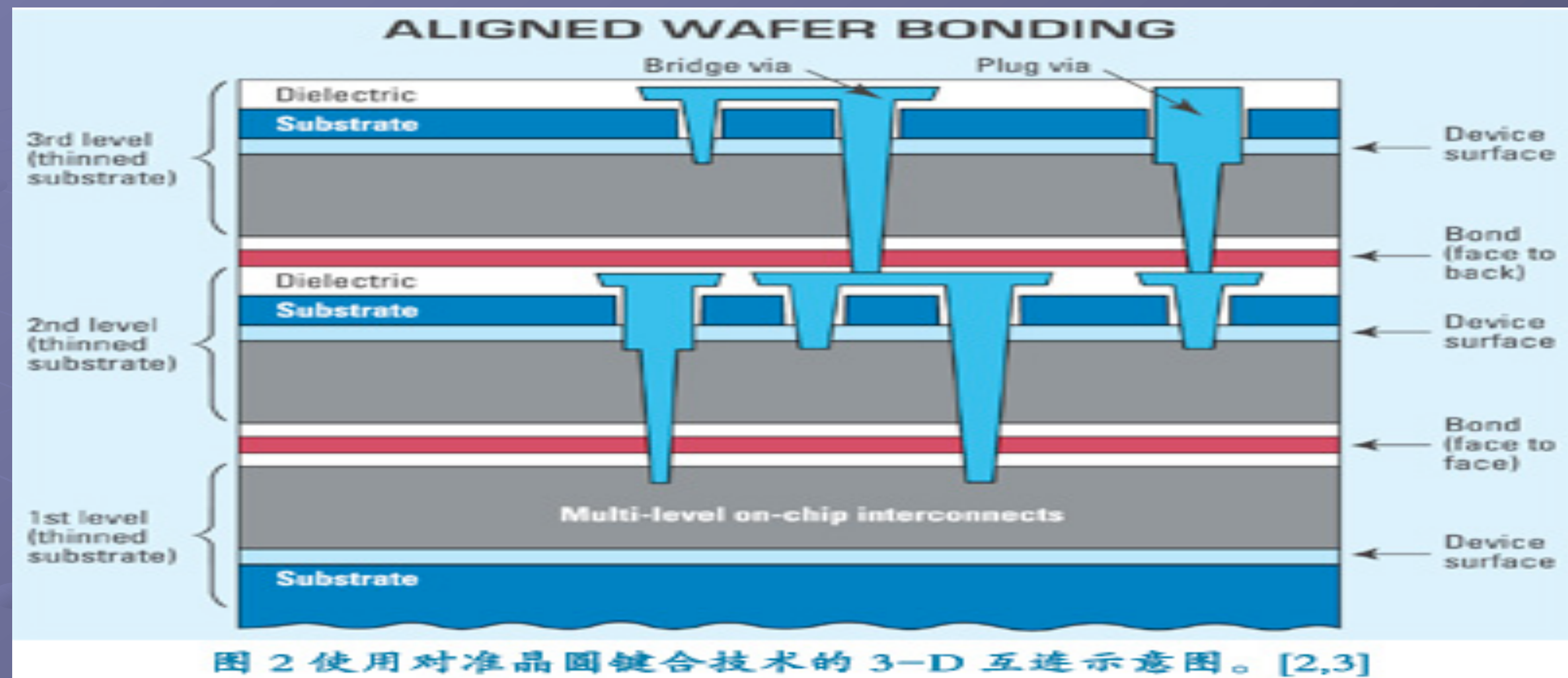


图 2 使用对准晶圆键合技术的 3–D 互连示意图。[2,3]

- Aligned Wafer Level Bonding can be described as process that allows stacking two or more processed wafers together involving, “the application of intermediary layer, wafer alignment and bonding” (Lindner, 1439).

Benefits of Aligned Wafer Bonding

- The benefits of device stacking are:
- “size reduction
- increase in “silicon efficiency
- reduction in signal delay
- reduced parasitic
- decrease in power consumption
- increase in speed
- increase in number of neighboring devices
- extension of bandwidth”

(Linder, 1439).

Intermediate Layers for Wafer Bonding

- An intermediate layer is necessary when bonding two wafers or substrates in wafer level alignment.
- There are seven different types of intermediate layers, "available for 3-D interconnection technology and wafer level packaging:
  - Solder alloys: requires low temperature and low force
  - Gold to gold wafer bonding: requiring high temperature and high force
  - Copper to copper wafer bonding: requiring high temperature and high force
  - Aluminum to aluminum wafer bonding: requiring reduced atmosphere (forming gas), high temperature and high force
  - Anodic bonding: requiring high temperature, high vacuum, high voltage
  - Silicon direct bonding (SDB): requires ultra clean bonding environment
  - Polymer bonding: requiring low temperature, low force, high vacuum" (Linder,1440).
- The various mechanical properties of the surface is vital to the viability of the process viscosity, thermal mismatch and fragility of the bonding elements should be considered.

Infrared Alignment:

- One of the first methods used in wafer alignment was Infrared Alignment.
- This method utilizes the infrared light for the alignment process.
- Silicon is, "transparent in the infrared spectrum, one can view and align both wafers to each other" (Mirza, 677)
- The limitations of using infrared imaging is diffraction, "alignment errors of +/- 5um"
- Transparency of the wafers may not be entirely clear due to composition of the wafer, particularly metal components that do not allow infrared light pass through (Mirza, 677).

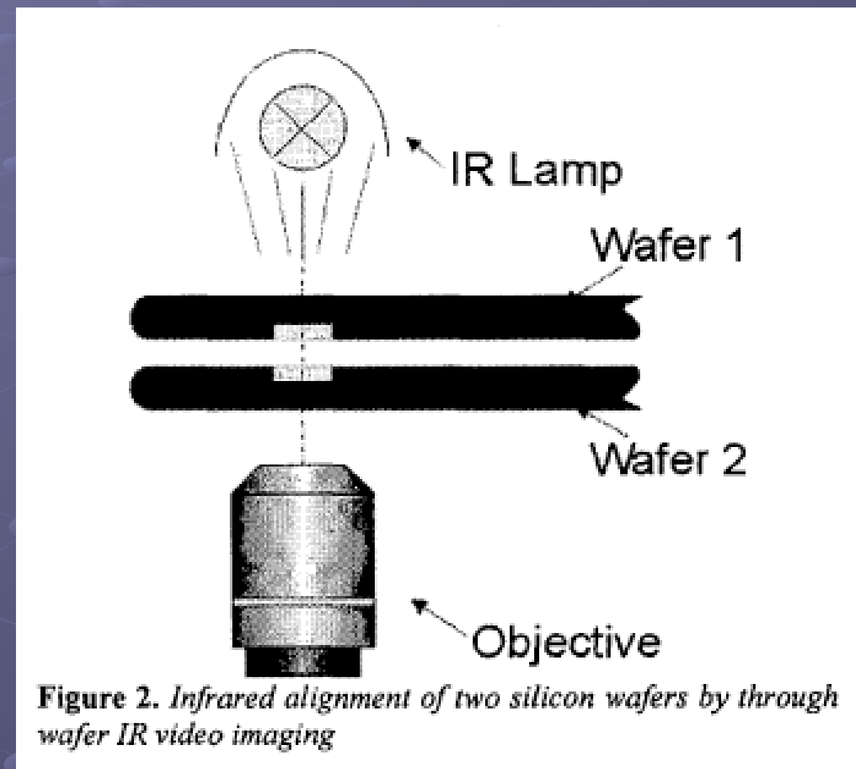


Figure 2. *Infrared alignment of two silicon wafers by through wafer IR video imaging*

Through Wafer Via Holes

- Etches an hole entirely through the first wafer to view the second wafer for the alignment process shown in figure 3.
- This process “requires precision registration of the backside via hole mask to the front side of the wafer”(Mirza, 677).
- This method is useful in MEMS applications where the thickness is several microns.

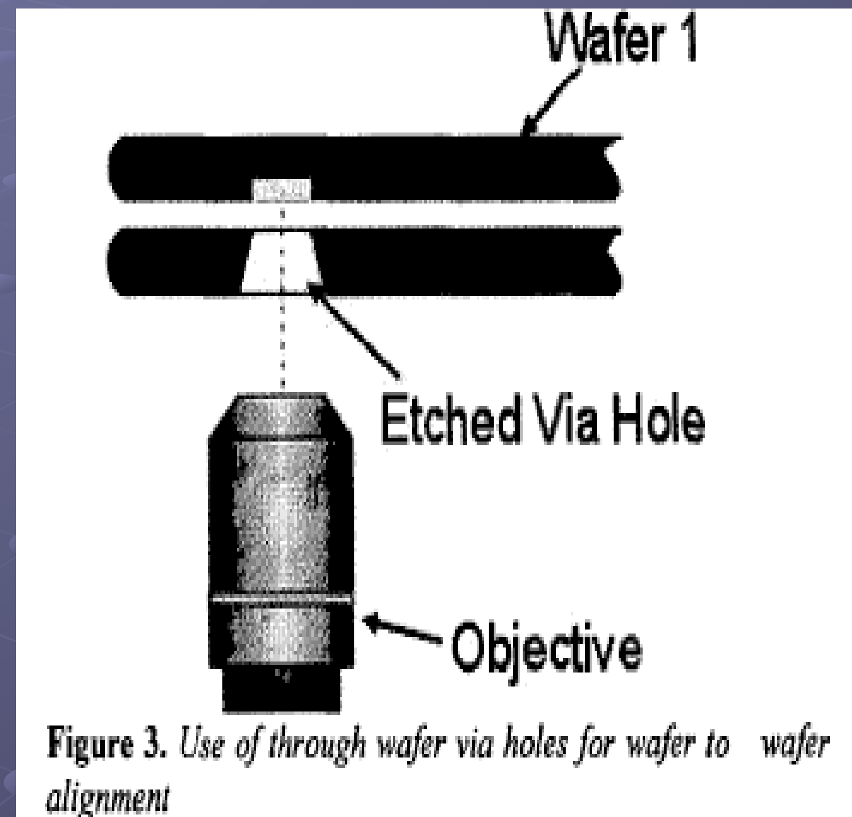


Figure 3. *Use of through wafer via holes for wafer to   wafer alignment*

Wafer Backside Alignment

- Utilizes alignment keys on the backside of the first wafer which are then aligned to the front side alignment marks of the second wafer, shown in figure 4.
- This method is, “a standard for MEMS wafer bonding.
- Requires precision registration precision registration of the backside alignment keys to the front side marks and exact alignment of the wafers.
- The registration of alignment keys and the aligning of both wafers, “each introduce errors of the order of 1 um” (Mirza, 678).
- Is acceptable for MEMS applications in the order of two or more microns.

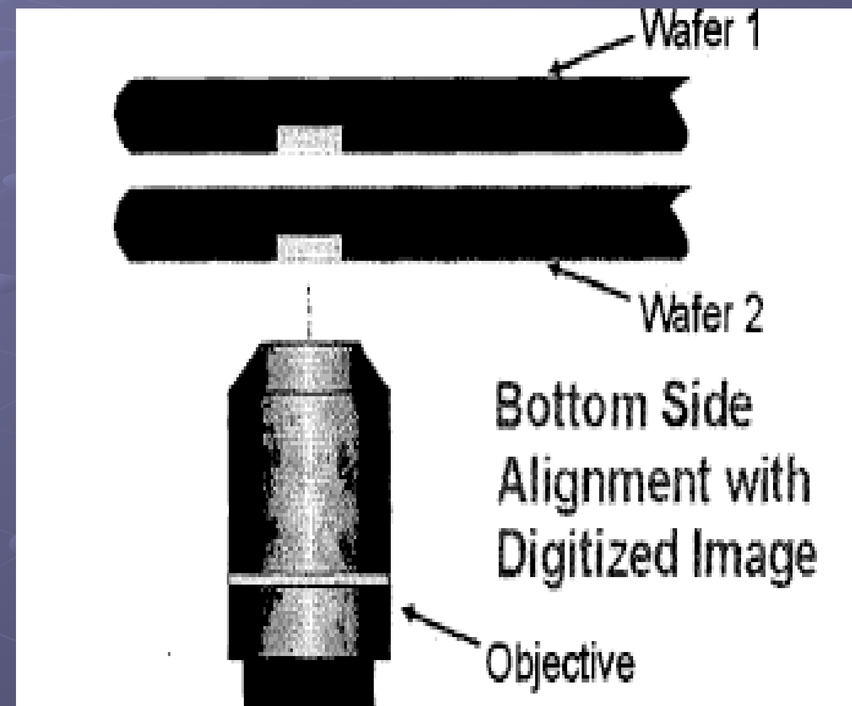
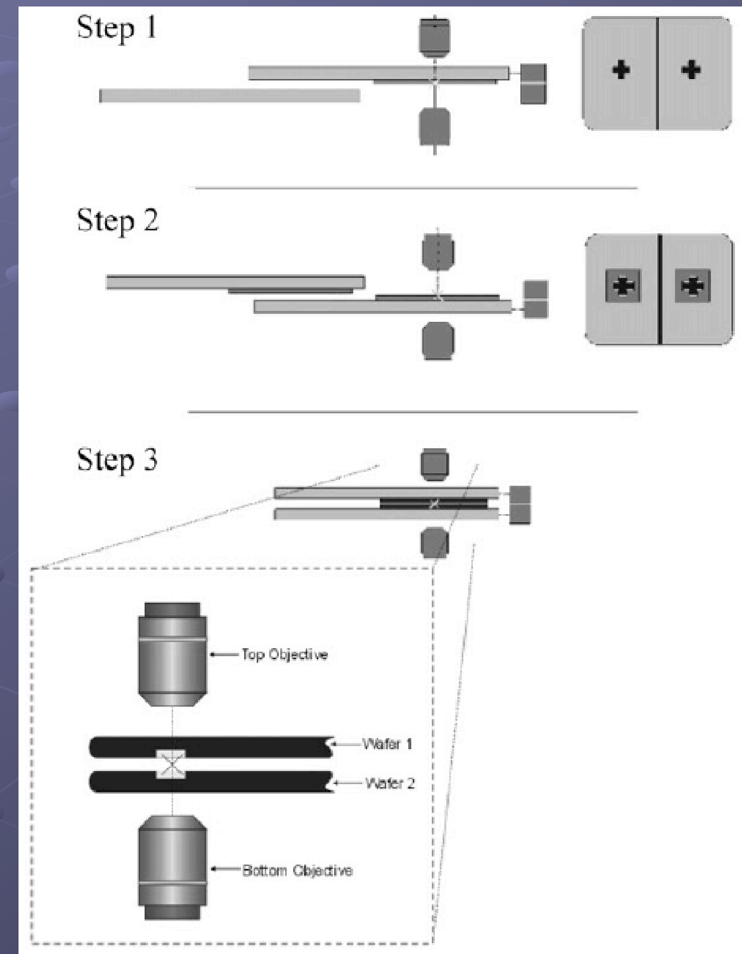


Figure 4: Wafer to wafer alignment using Wafer Backside Alignment Keys.

Face to Face Alignment: Using SmartView

- Utilizes two microscopes for alignment, one above and one below the wafer stack.
- The two microscopes, “system focuses on a common axis calibrated for each alignment.
- Each microscope objective observes one alignment key on the surface of the wafer”
- Each microscope digitally stores the alignment key of the farthest wafer then aligns the wafers according to the digital alignment keys (Dragoi, 426).
- Both wafer alignment stages, “uses encoded stage motors that allow X,Y movements of 0.1 micron” (Mirza, 679).



Face to Face Alignment: Using SmartView

- Both wafer alignment stages, “uses encoded stage motors that allow X,Y movements of 0.1 micron” (Mirza, 679).
- The face to face alignment method is able to, “achieve 1 micron alignment precision” (Dragoi, 425).
- This process also has an “repeatability of the measurement system is less than 0.35 microns”(Dragoi, 426).
- Smart View, can be a completely automated system or a semi automated system.
- Face to face alignment is the most accurate alignment available and is completely viable in a commercial process.

Wafer Bonding

- Intermediate bonding layers are either spun or sprayed on for uniformity of the layers.
- Sprayed bonding agents such as polymers, “average uniformity achieved was 7.5%”(Lindner, 1440).
- The process of forming the interconnects and bonding the wafers is shown below in figure 6.
- The usual thinning process procedures are: “mechanical grinding, lapping, reactive ion etching (RIE), wet etching, ADP-DCE (Atmospheric Down Stream Plasma Dry Chemical Etching)” (Lindner,1441). After thinning both the top and back side of the resulting wafer stacks.

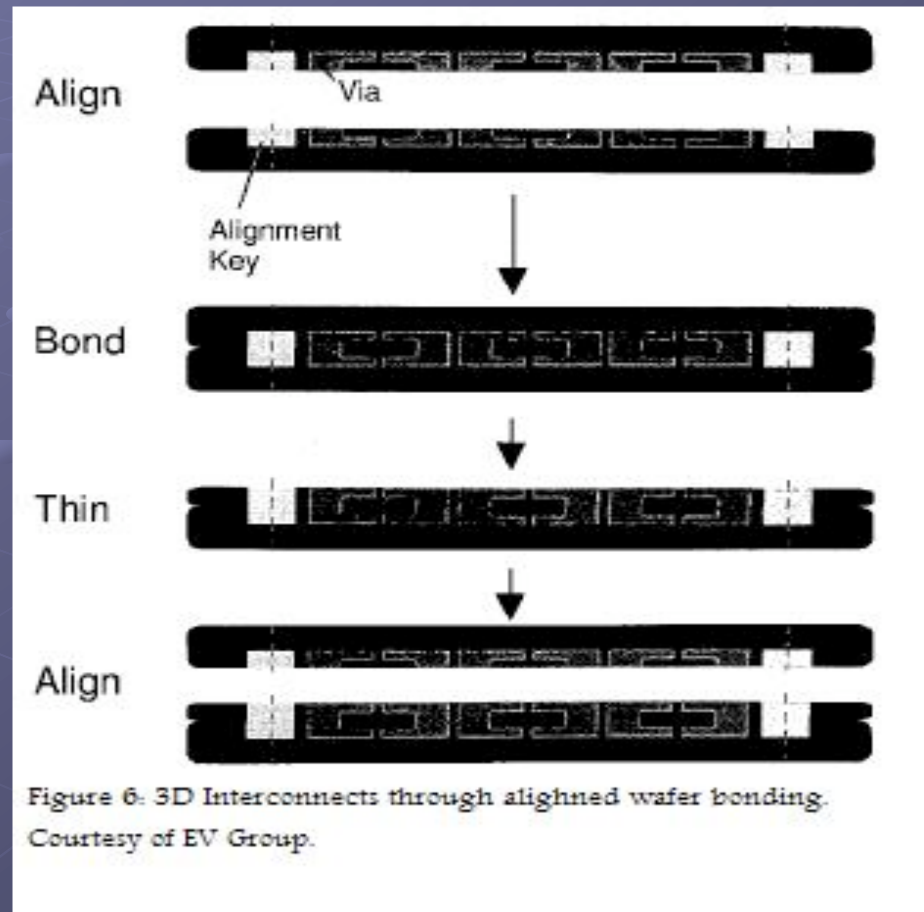
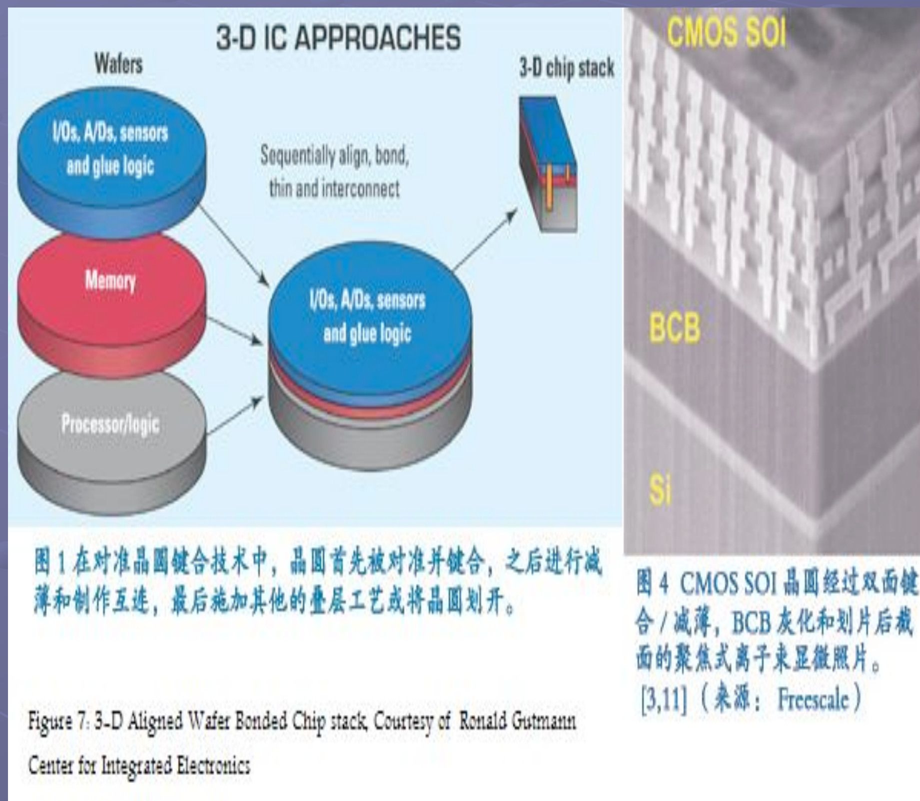
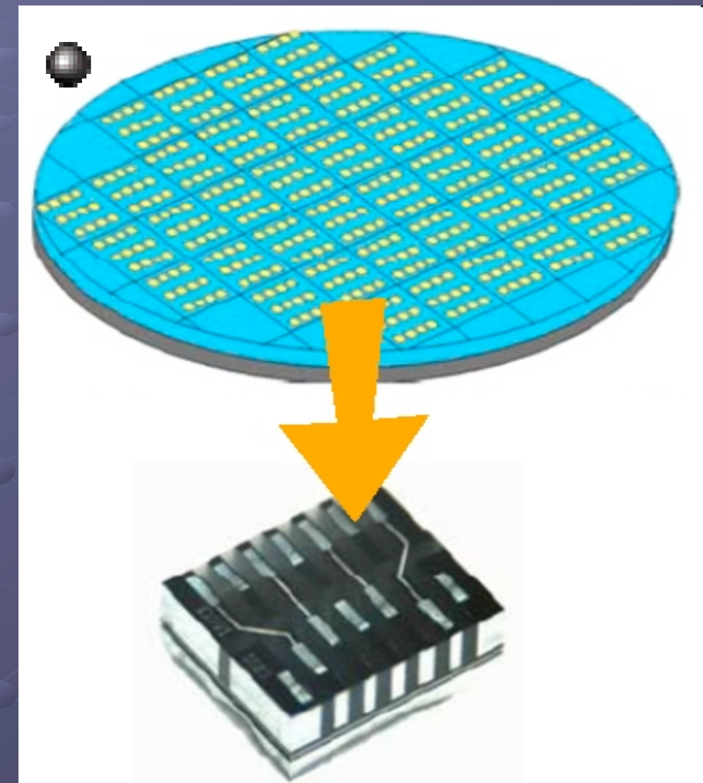


Figure 6: 3D Interconnects through alighned wafer bonding. Courtesy of EV Group.

Applications





Capping wafer with planar surface and multiple feed-trough and picture of a MEMS device sample - Courtesy of VTI

References

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