Aligned Wafer Level Bonding

The following paper will cover the concepts, issues and applications of aligned wafer level bonding. There are will be an overview of five different methods for wafer level bonding: infrared alignment, wafer backside, through wafer via holes, wafer backside alignment and face to face alignment. Each method uses similar methods to attain the same goal but have limitations when it comes to alignment.

Aligned Wafer Level Bonding can be described as a process that allows stacking two or more processed wafers together involving, “the application of intermediary layer, wafer alignment and bonding” (Lindner, 1439). This process is used in Wafer Level Packaging and 3-D Interconnection technologies. The benefits of device stacking are, “size reduction, increase in “silicon efficiency”, reduction in signal delay, reduced parasitic, decrease in power consumption, increase in speed, increase in number of neighboring devices and extension of bandwidth” (Linder, 1439). The continuing need for smaller devices such as cell phones, PDA, camcorders, cameras, laptops, flash drives, scan disks requires new ways of designing and producing smaller, faster, more efficient processors for volume large scale production.

Intermediate Layers for Wafer Bonding:

An intermediate layer is necessary when bonding two wafers or substrates in wafer level alignment. There are seven different, major intermediate layers types, “available for 3-D interconnection technology and wafer level packaging:

1. Solder alloys, requires low temperature and low force
2. Gold to gold wafer bonding, requiring high temperature and high force
3. Copper to copper wafer bonding, requiring high temperature and high force
4. Aluminum to aluminum wafer bonding, requiring reduced atmosphere (forming gas), high temperature and high force
5. Anodic bonding, requiring high temperature, high vacuum, high voltage
6. Silicon direct bonding (SDB), requires ultra clean bonding environment
7. Polymer bonding, requiring low temperature, low force, high vacuum” (Linder, 1440).

When choosing an intermediate layer the surface of the processed wafers must be taken into consideration. The various mechanical properties of the surface are vital to the viability of the process, thermal mismatch and fragility of the bonding elements should be considered. Polymer bonding is less likely to damage the wafers since it is a low temperature, low force compared to the various other metal to metal wafer bonds.

Infrared Alignment:

One of the first methods used in wafer alignment is Infrared Alignment. This method utilizes the infrared light for the alignment process. Silicon is, “transparent in the infrared
spectra, one can view and align both wafers to each other” (Mirza, 677). As seen in Figure 2 below, an objective is placed under the two wafers using the alignment marks, similar to aligning different mask layers used on the wafers before they are processed. The limitations of using infrared imaging is diffraction, “alignment errors of +/- 5um isn’t uncommon” also the transparency of the wafers may not be entirely clear due to composition of the wafer, particularly metal components that do not allow infrared light pass through (Mirza, 677).

Through Wafer Via Holes:

Through wafer via holes etches a hole entirely through the first wafer to view the second wafer for the alignment process shown in figure 3 on the previous page. This process “requires precision registration of the backside via hole mask to the front side of the wafer”(Mirza, 677). This method is useful in MEMS applications since the thickness of most MEMS are several microns.

Wafer Backside Alignment:

Wafer backside alignment utilizes alignment keys on the backside of the first wafer which are then aligned to the front side alignment marks of the second wafer, shown in figure 4 below. This method is, “a standard for MEMS wafer bonding, [which] requires precision registration precision registration of the backside alignment keys to the front side marks [and] the two wafers must be exactly aligned to each other based on these backside alignment keys”(Mirza, 678). The registration of alignment keys and the aligning of both wafers, “each introduce errors of the order of 1 um” which is acceptable for MEMS applications in the order of two or more microns(Mirza, 678).

Face to Face Alignment: Using SmartView

Face to face alignment utilizes two microscopes for alignment, one above and one below the wafer stack. The two microscopes, “system focuses on a common axis calibrated for each
alignment. Each microscope objective observes one alignment key on the surface of the wafer. Each microscope digitally stores the alignment key of the farthest wafer then aligns the wafers according to the digital alignment keys (Dragoi, 426). Both wafer alignment stages, “uses encoded stage motors that allow X,Y movements of 0.1 micron” (Mirza, 679). The face to face alignment method is able to, “achieve 1 micron alignment precision” (Dragoi, 425). This process also has a “repeatability of the measurement system is less than 0.35 microns” (Dragoi, 426). Face to face alignment is the most accurate alignment available and is completely viable in a commercial process. The machine used in face to face alignment is the Smart View, which can be a completely automated system or a semi automated system.

**Wafer Bonding:**

The intermediate bonding layers are either spun or sprayed on for uniformity of the layers, sprayed bonding agents such as polymers, “average uniformity achieved was 7.5%” (Lindner, 1440). The process of forming the interconnects and bonding the wafers is shown below in figure 6. The usual thinning process procedures are: “mechanical grinding, lapping, reactive ion etching (RIE), wet etching, ADP-DCE (Atmospheric Down Stream Plasma Dry Chemical Etching)” (Lindner, 1441). After thinning both the top and back side of the resulting wafer stacks, the process is complete.

![3-D IC APPROACHES](image)

This paper covered the concepts of aligned wafer level bonding: intermediary layer, wafer alignment. This paper also discussed the limitations of five different techniques issues used in aligned wafer bonding. Lastly applications of aligned wafer level bonding were discussed in the beginning of the paper, which included devices for cell phones, laptops, camcorders, cameras, flash drives, and scan disks.
Reference:


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