

Basic Computer Organization Topics

- I. Instruction Set Architectures
 - A. Machine state (visible portion or programmer's view of the architecture)
 - 1. Memory organization
 - 2. Register organization
 - 3. Data types
 - 4. Interrupts and events
 - B. Register organizations
 - 1. Accumulators
 - 2. Index Registers
 - 3. General Purpose Registers (GPRs)
 - 4. Load-store machines
 - 5. Stack machines
 - C. Instruction types
 - 1. Operations (arithmetic, logical operations, etc.)
 - 2. Data movement (load / store)
 - 3. Control flow
 - D. Data types
 - 1. Consists of a data representation, and a set of operations on the representation
 - 2. Ex: integer, floating point (single and double precision), narrow width fixed point, etc.
 - E. Addressing Modes
 - 1. Big vs. little endian
 - 2. Register
 - 3. Immediate
 - 4. Direct
 - 5. Register indirect
 - 6. Displacement
 - 7. Indexed
 - F. Instruction Encoding
 - 1. Fixed instruction formats
 - 2. Variable-length instructions
 - 3. Compromise: a small number of instruction lengths
 - G. Control
 - 1. Unconditional jumps
 - 2. Conditional jumps (branches)
 - 3. Conditions (condition codes, flags, registers)
 - 4. Support for procedures
 - 5. Support for exceptions
 - H. RISC vs CISC
- III. Pipelining
 - A. Implementing an ISA
 - 1. Computer architecture building blocks
 - 2. Pipeline implementation of MIPS

- a. Stages (F,R,E,M,W)
 - b. Pipeline registers
 - c. Computing pipeline performance
- B. Structural hazards
- C. Data hazards
 - 1. Types (RAW,WAW,WAR)
 - 2. Pipeline stall
 - 3. Bypass (forwarding)
- D. Control hazards
 - 1. Pipeline stall
 - 2. Early branch test and target calculation
 - 3. Static prediction
 - 4. Delayed branch
- E. Exceptions
 - 1. Types (synchronous, asynchronous)
 - 2. Restartability
 - 3. Precise semantics
 - 4. Problems with synchronous exceptions
 - a. Multiple exceptions
 - b. Out-of-order exceptions
 - 5. Single commit point
- F. Multi-cycle operations
 - 1. Bandwidth, latency
 - 2. Impact on pipeline
 - a. New structural hazards (competing for writeback port)
 - b. More forwarding paths
 - c. New data hazards that must stall
 - d. Complications for precise interrupts