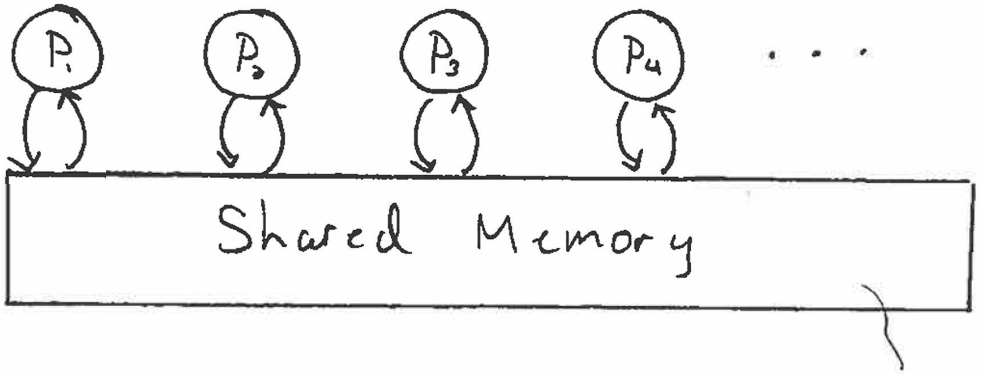
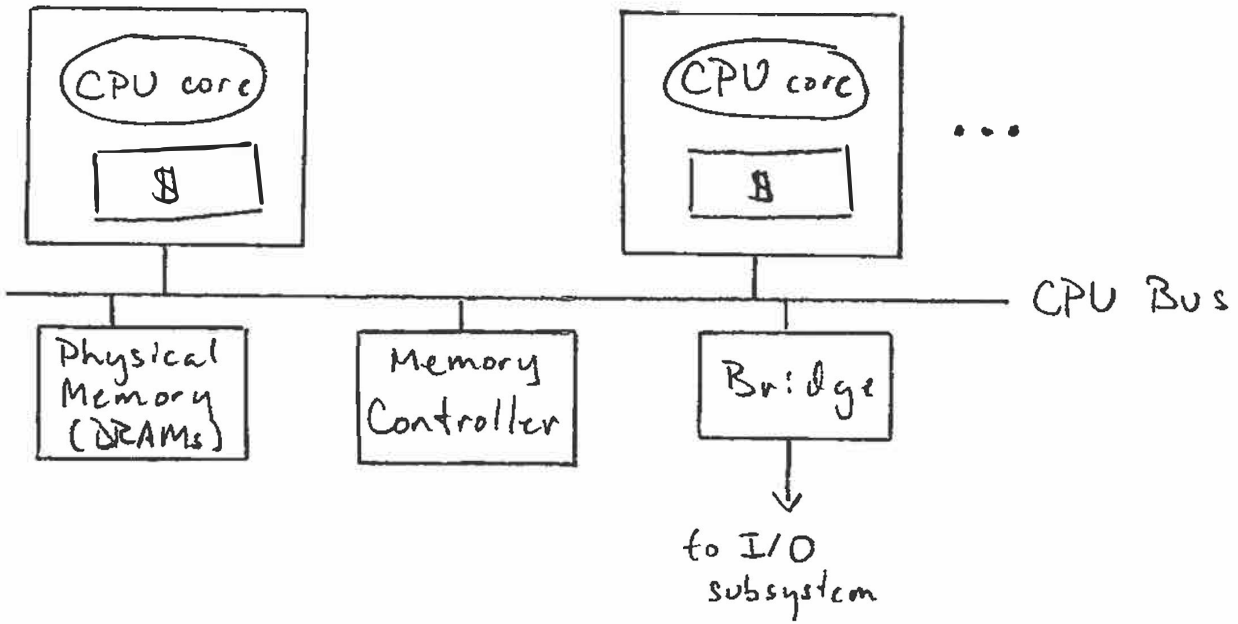
Bus-Based Multiprocessors

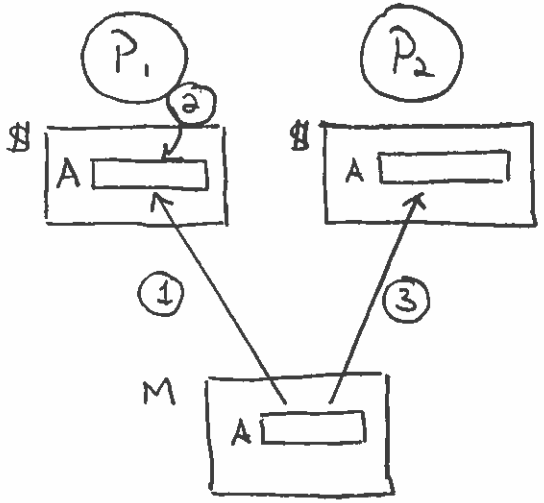
Shared Memory Model:



Shared Memory Implementation:



Cache Coherence Problem



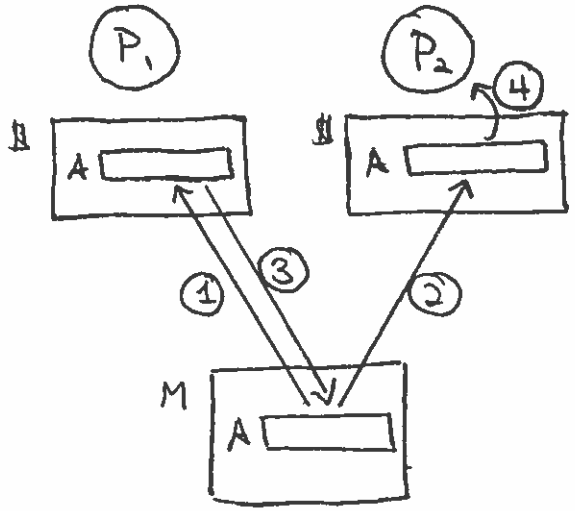
(Assume writeback caches)

① P_1 performs ld A

② P_1 performs st A
⇒ A is dirty in P_1's cache

③ P_2 performs ld A

⇒ P_2 loads stale copy of A from memory.



(Assume write through caches)

① P_1 performs ld A

② P_2 performs ld A

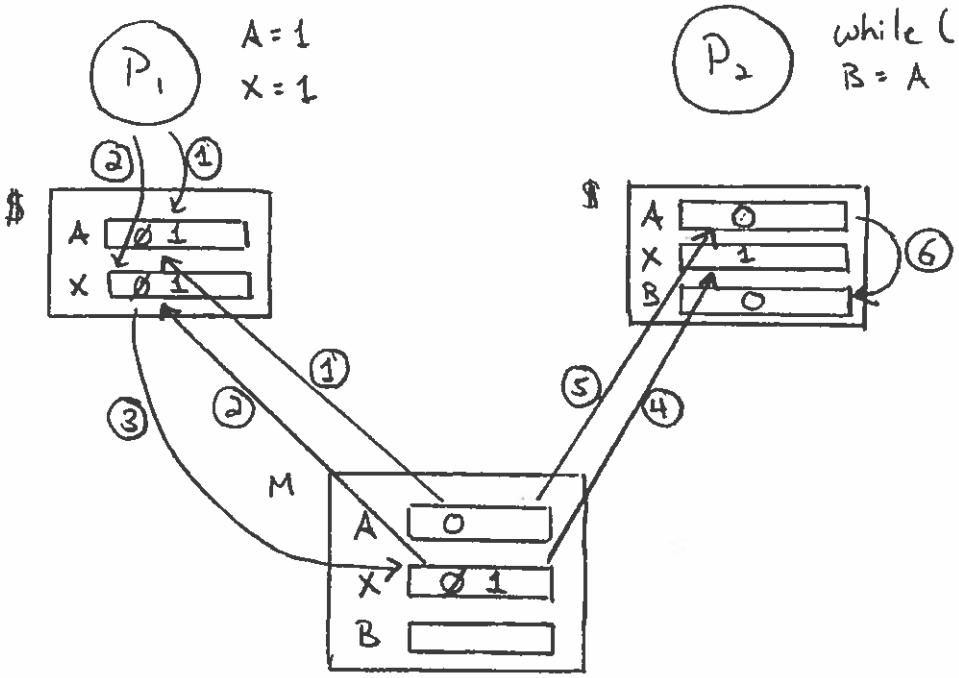
③ P_1 performs st A

④ P_2 performs ld A

⇒ P_2 loads stale copy of A from cache.

Memory Consistency Model

⇒ When sequential consistency is broken.



Sequentially consistent order:

- P_1 writes A = 1
- P_1 writes X = 1
- P_2 reads X = 1
- P_2 reads A = 1
- P_2 writes B = A = 1

⇒ Caches reorder writes.

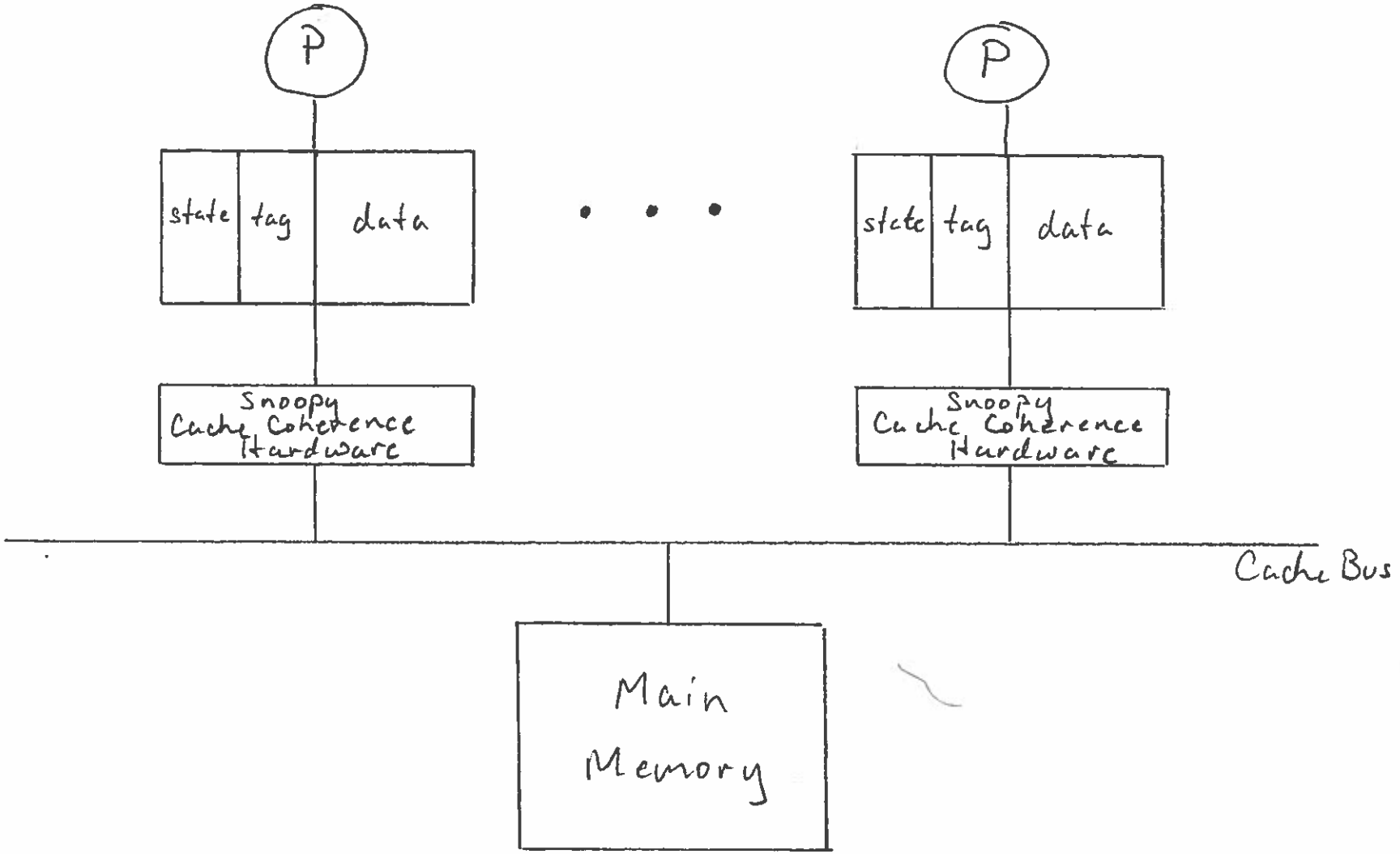
P_1 order: A = 1, X = 1

P_2 order: X = 1, A = 1

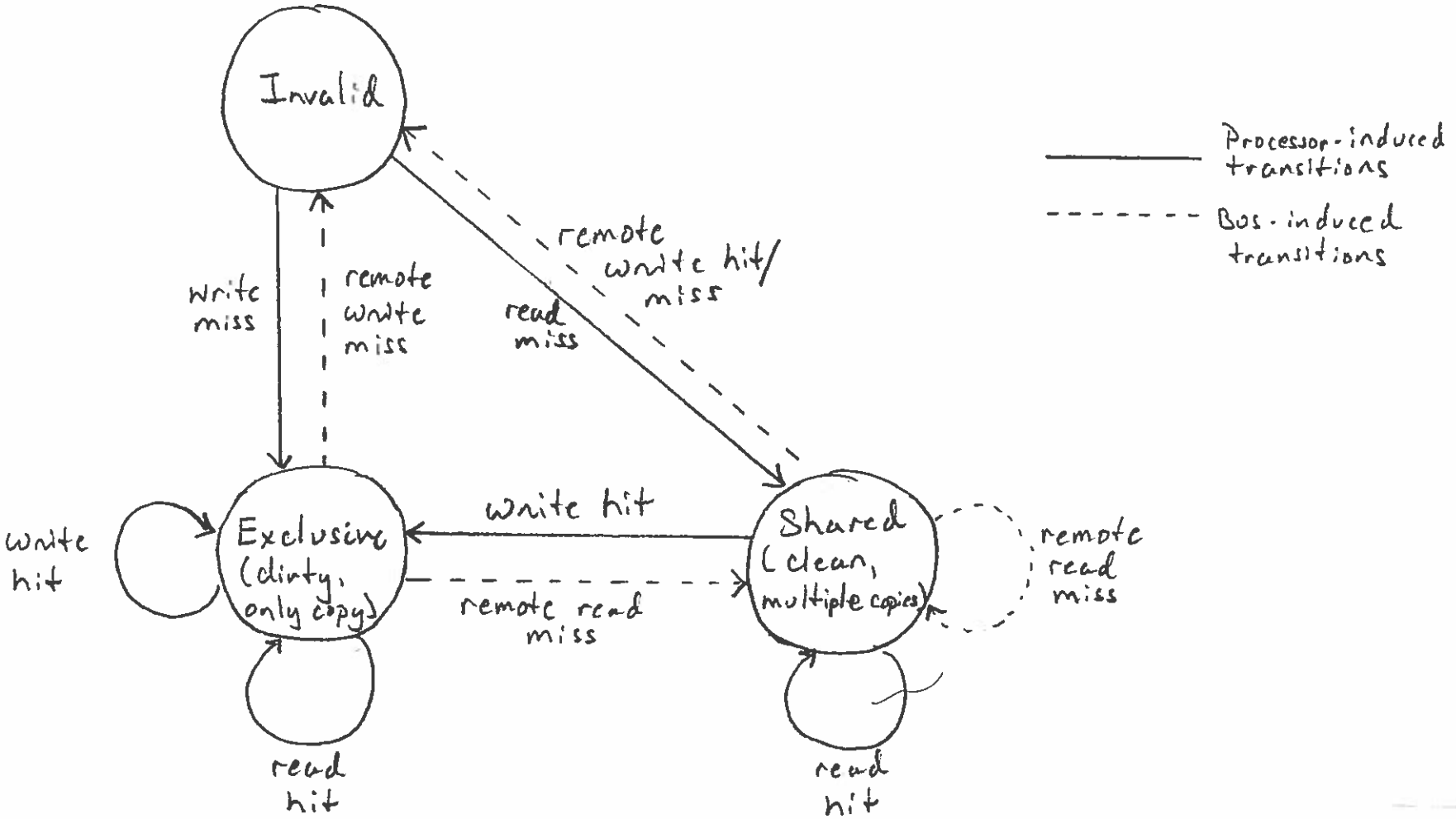
Assume write back caches

1. P_1 writes A = 1
2. P_1 writes X = 1
3. X is written back to memory
4. P_2 reads X = 1
5. P_2 reads A = 0
6. P_2 writes B = A = 0

Snoopy Cache-Coherence Buses



Bus-Based Write Invalidate



Bus-Based MESI