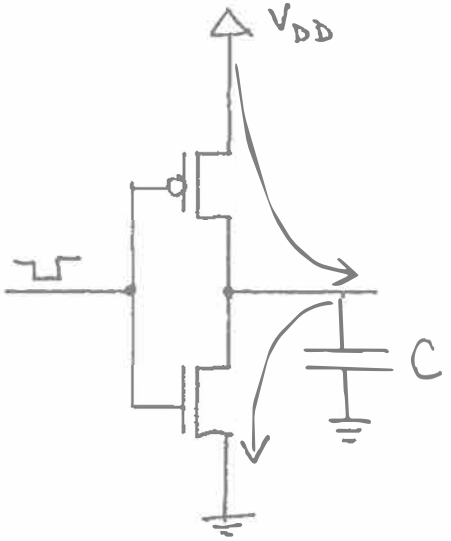
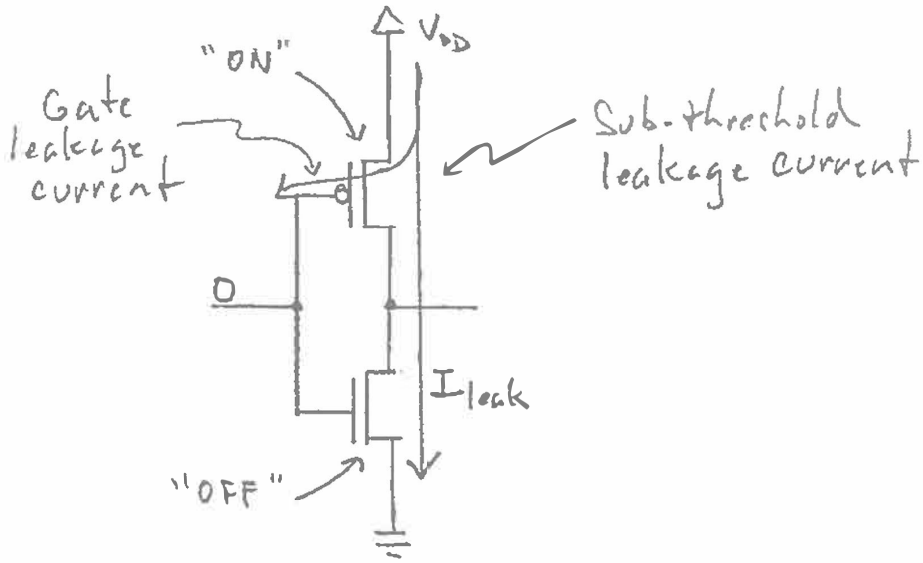
Power Consumption in CMOS





Dynamic Power: due to switching

$$P_D = [(C \cdot V_{DD}) f a] V_{DD}$$
$$= C V_{DD}^2 f a$$

Static Power: due to leakage

$$P_S = I_{leak} \cdot V_{DD}$$
$$I_{leak} = k_1 e^{-\frac{q V_T}{a \cdot k_2 T}}$$

Scaling V_{DD} and Leakage

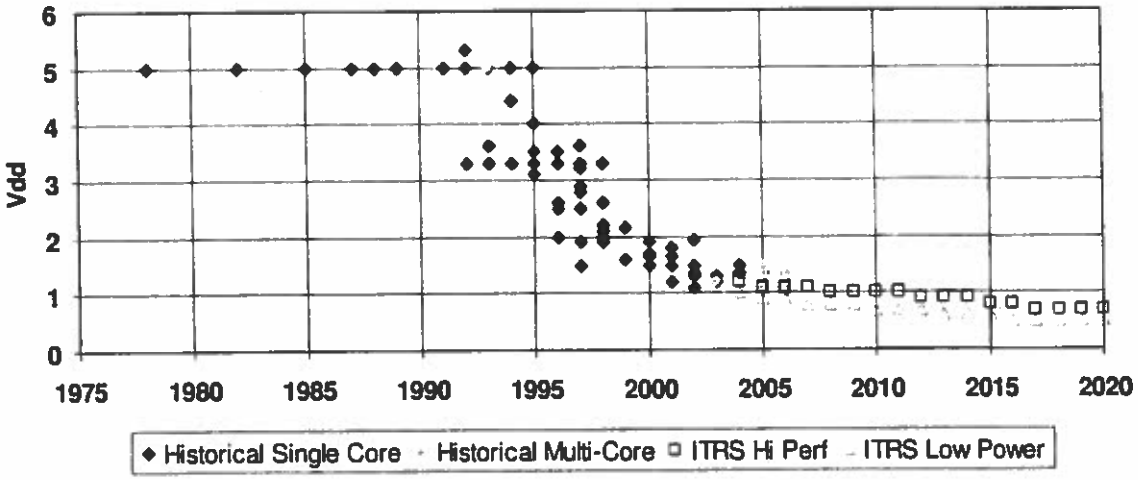
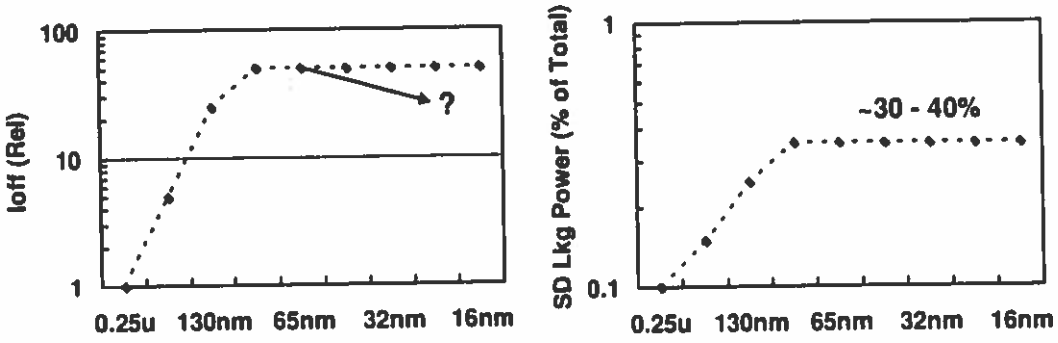


Figure 4.7: Microprocessor V_{dd}.

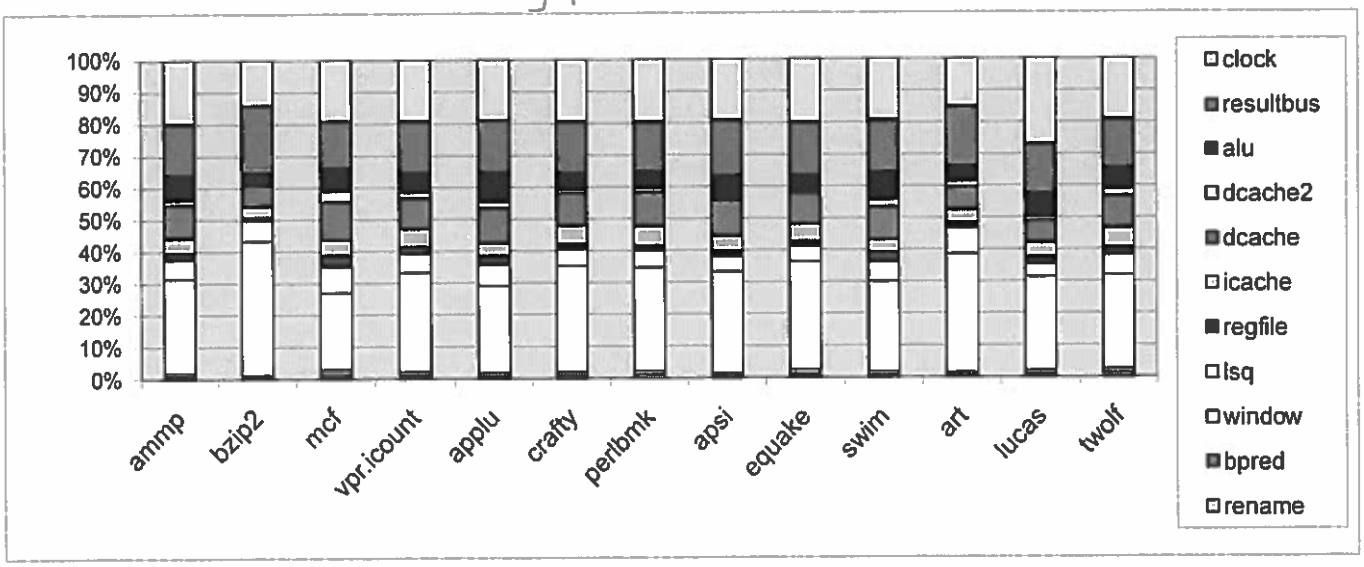


Sub-leakage current and leakage power fraction of total power as a function of feature size

Data from Kogge et al. "ExaScale Computing Study: Technology challenges in Achieving Exascale Systems" 2008.

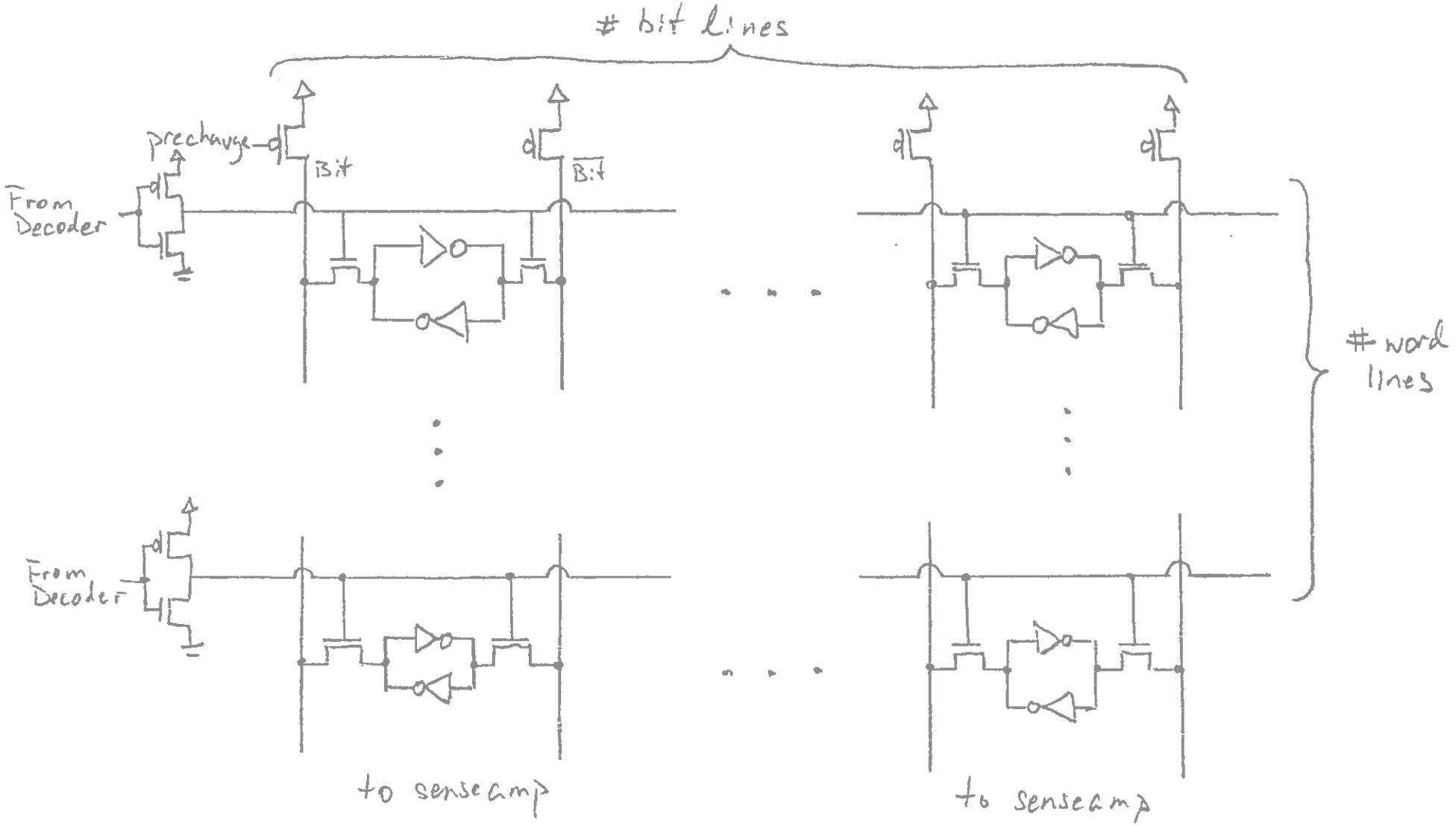
Power Breakdown in an Out-of-Order Superscalar Processor

Processor:
- 8-way issue
- 256-entry ROB
- 128-entry conflict queue
- L1 Cache: Split 64KB 2-way set associative
- L2 Cache: Unified 1 MB 4-way set associative
- 8K-entry branch predictor
- 9 integer functional units
- 6 floating point functional units.

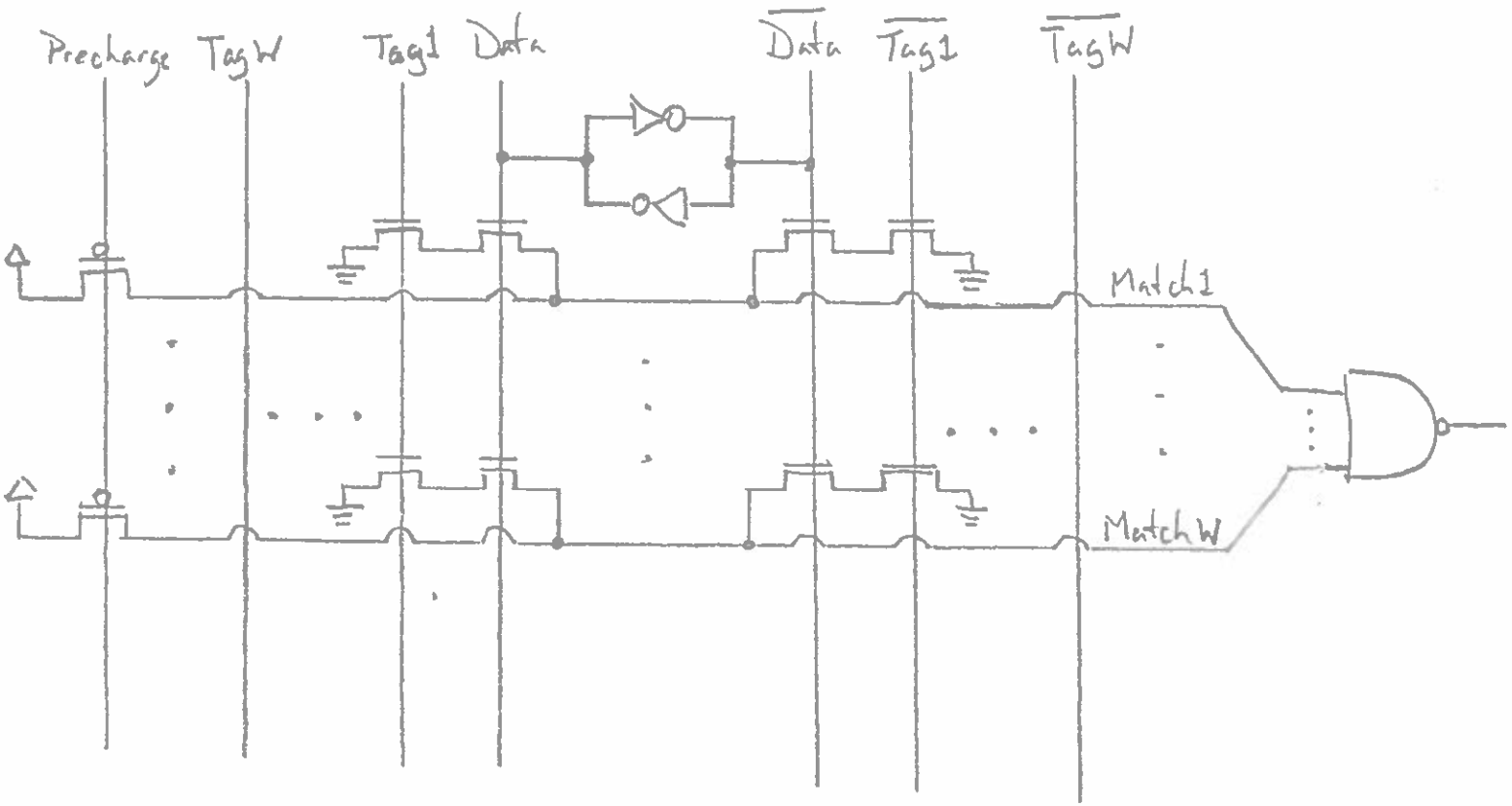


Benchmarks from SPEC CPU2000 suite.

Power Estimation for SRAM Arrays



Power Estimation for CAM Arrays



Match Lines ⇐ Word Lines

Tag Lines ⇐ Bit Lines