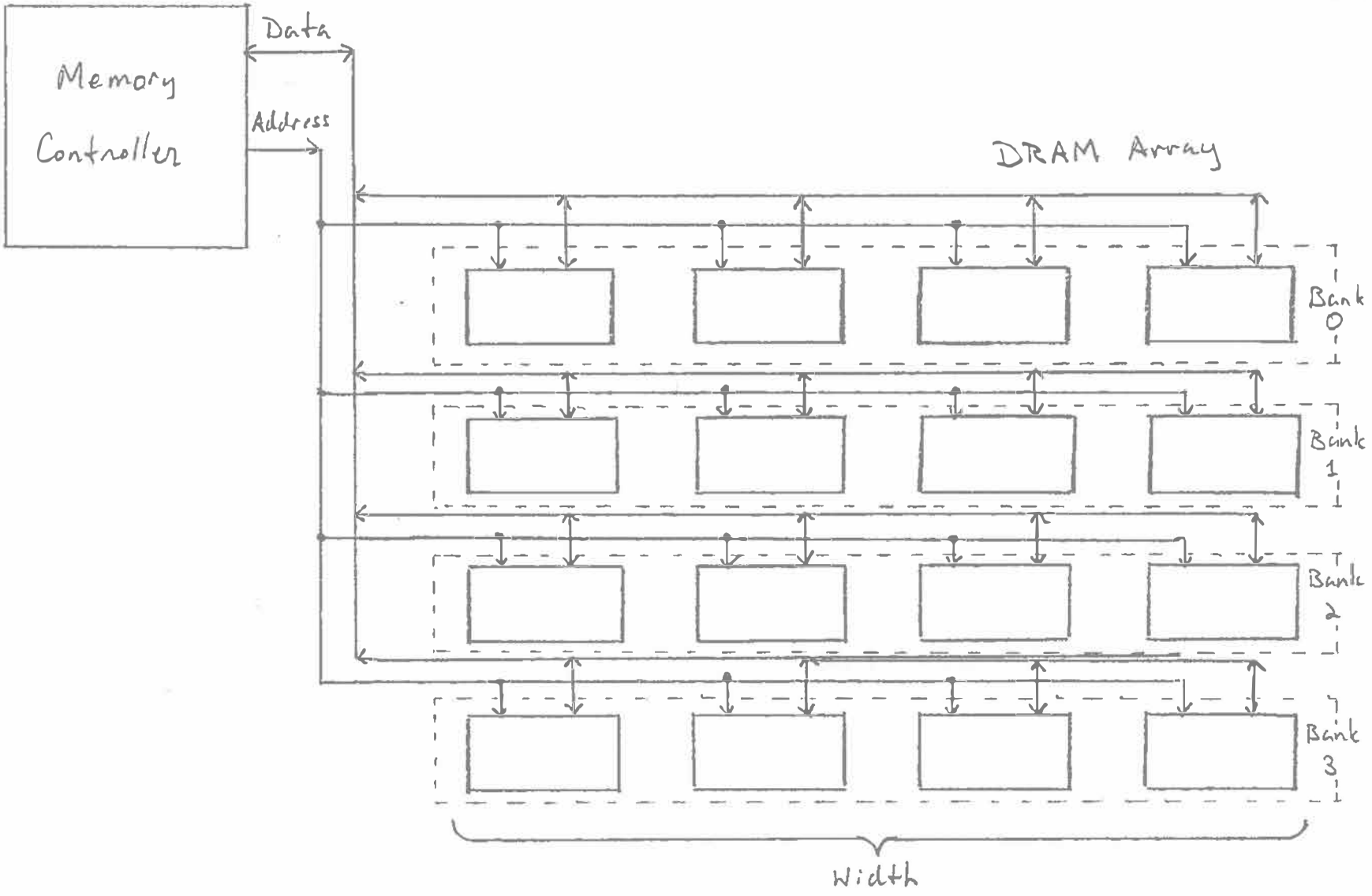
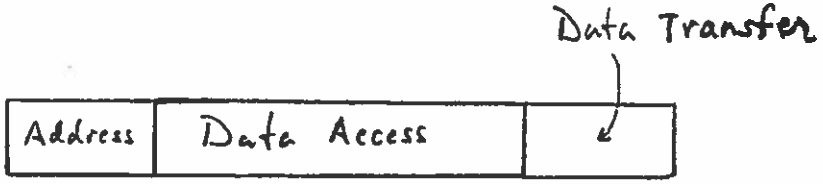
Memory Subsystem Architecture



Memory Transaction

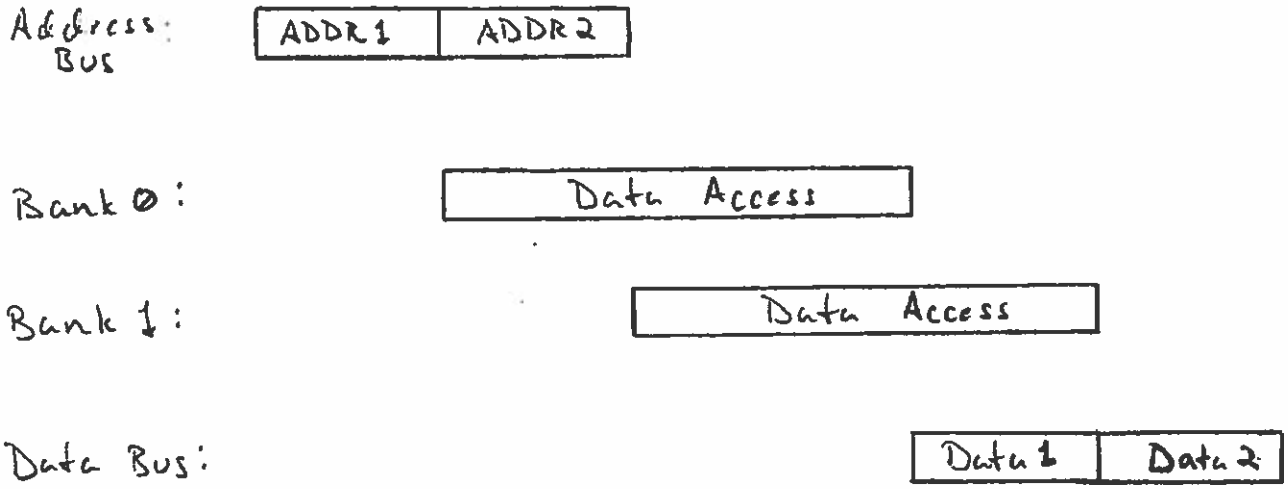
Single Memory Access:



Ex: $t_{ADDRESS} = 10ns$
$t_{data\_access} = 50ns$
$t_{data\_transfer} = 10ns$

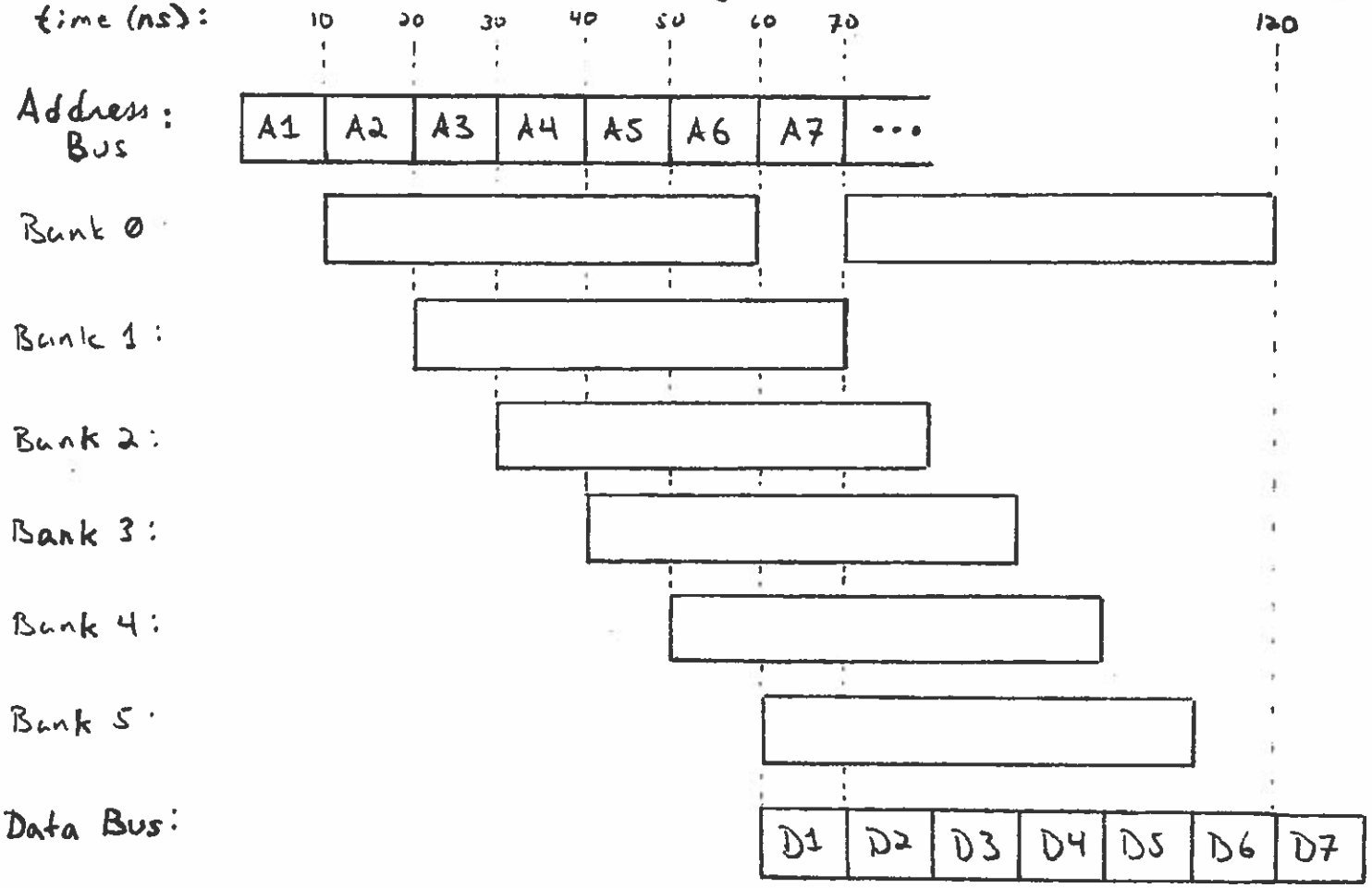
} Total access latency = 70ns

Interleaved Memory Access:



Low Order Interleaving

How many banks are needed?



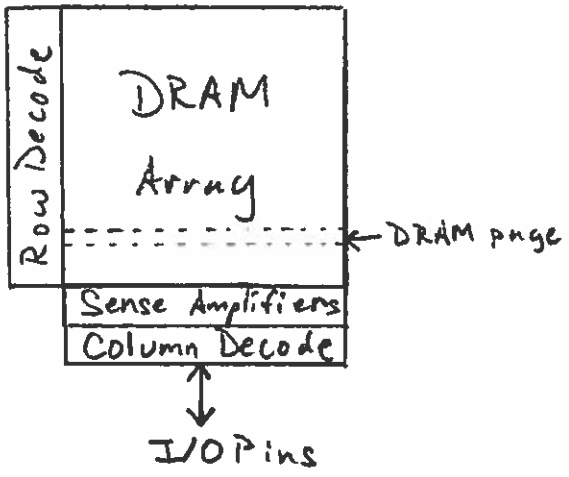
DRAM Architecture

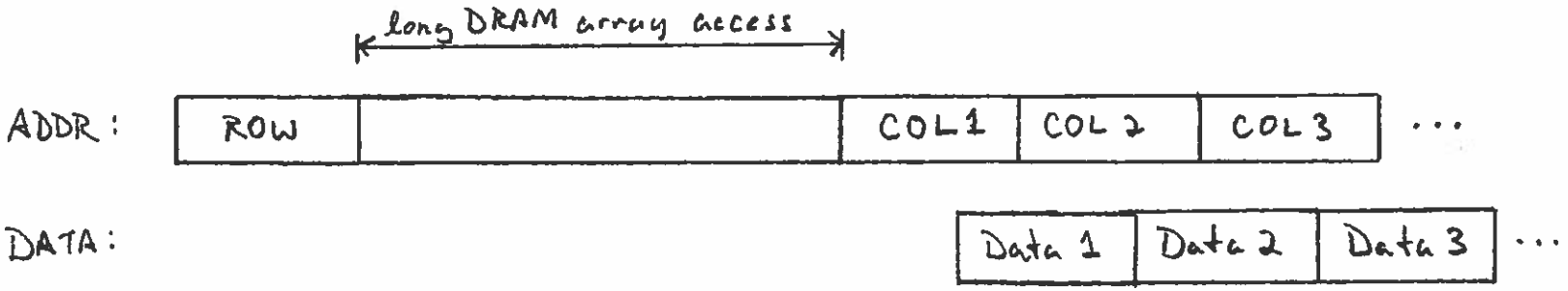
EDO DRAM:

DRAM page size typically the square root of DRAM size

e.g 64 Mbit DRAM ⇒ 8 Kbits = 1 Kbytes

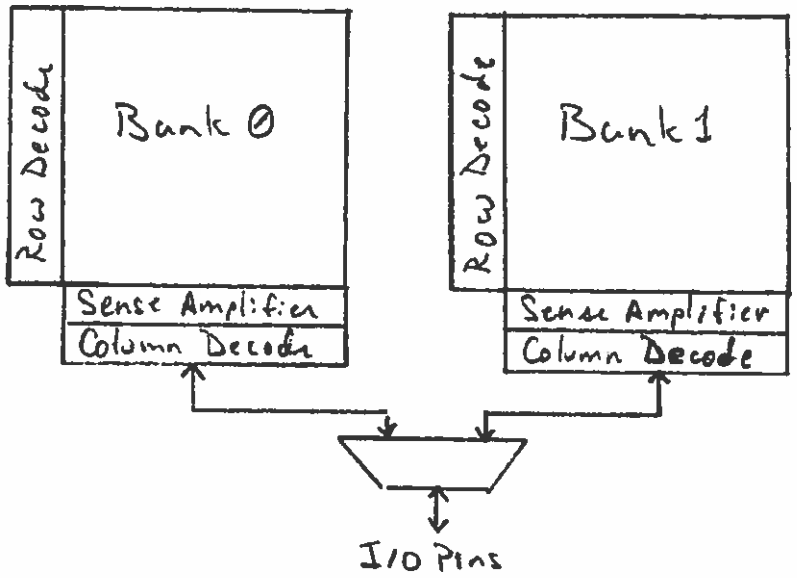
lots of data in a DRAM page





DRAM Architecture

Multiple internal banks:



CDRAM: