

Loop Unrolling Ex. 1 (Parallel Loop)

for ($i=0$; $i < n$; $i++$)
 $d[i] = a[i] * b[i] + c$

LOOP: L.D F0, (R1)
 L.D F2, (R2)
 DADDI R1, #8
 DADDI R2, #8
 MUL.D F4, F0, F2
 ADD.D F6, F4, F8
 S.D F6, (R3)
 DADDI R3, R3, #8
 DADDI R4, R4, #1
 SLT R5, R4, R6
 BNEZ R5, LOOP

R1 - $\&(a[i])$
R2 - $\&(b[i])$
R3 - $\&(d[i])$
R4 - i
R6 - n
F8 - c

Loop Unrolling Ex. 1

(Parallel Loop)

```
for (i=0; i<n; i+=2) {  
    a[i] = a[i] * b[i] + c;  
    a[i+1] = a[i+1] * b[i+1] + c;  
}
```

```
LOOP: L.D F0, (R1)  
      L.D F2, (R2)  
      MUL.D F4, F0, F2  
      ADD.D F6, F4, F8  
      S.D F6, (R3)  
-----  
      L.D F0, 8(R1)  
      L.D F2, 8(R2)  
      MUL.D F4, F0, F2  
      ADD.D F6, F4, F8  
      S.D F6, 8(R3)  
      DADDI R1, R1, #16  
      DADDI R2, R2, #16  
      DADDI R3, R3, #16  
      DADDI R4, R4, #2  
      SLT R5, R4, R6  
      BNEZ R5, LOOP
```

Loop Unrolling Ex 1 (Parallel Loop)

```
LOOP: L.D F0, (R1)
      L.D F2, (R2)
      L.D F10, 8(R1)
      L.D F12, 8(R2)
      DADDI R1, R1, #16
      DADDI R2, R2, #16
      MUL.D F4, F0, F2
      MUL.D F14, F10, F12
      ADD.D F6, F4, F8
      ADD.D F16, F14, F8
      S.D F6, (R3)
      S.D F16, 8(R3)
      DADDI R3, R3, #16
      DADDI R4, R4, #2
      SLT R5, R4, R6
      BNEZ R5, LOOP
```

Loop Unrolling Ex 2 (Sequential Loop)

```
max = a[0];  
for (i=1; i<n; i++)  
    if (a[i] > max)  
        max = a[i];
```

```
R2 = &a[i]  
R4 = i  
R8 = max  
R9 = n
```

```
LOOP: LD R1, (R2)  
      SGT R3, R1, R8  
      BEQZ R3, NOMAX  
      DADD R8, R1, R0  
      DADDI R2, R2, #4  
      DADDI R4, R4, #1  
      SLT R5, R4, R9  
      BNEZ R5, LOOP
```

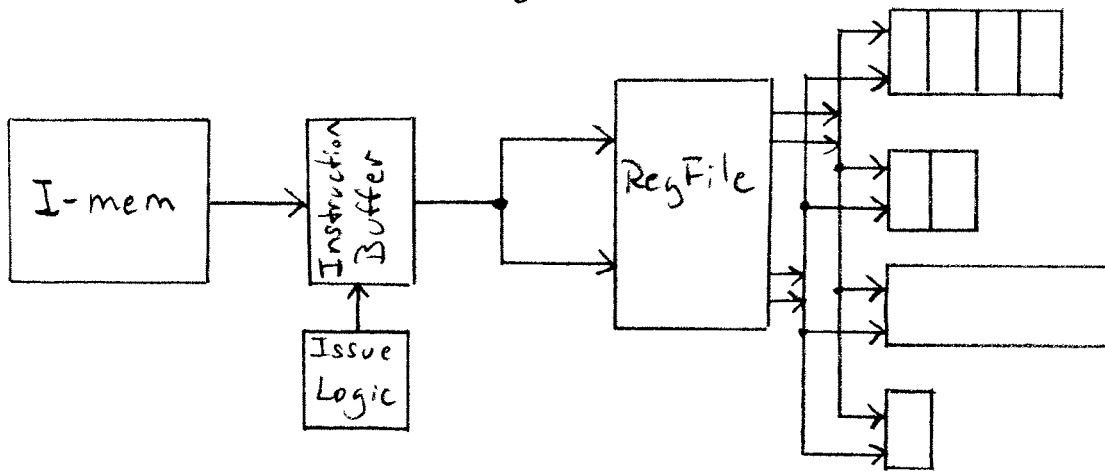
Loop Unrolling Ex. 2 (Sequential Loop)

```
LOOP: LD R1, (R2)
      SGT R3, R1, R8
      BEQZ R3, NOMAX1
      DADD R8, R1, R0

NOMAX1: LD R1, 4(R2)
        SGT R3, R1, R8
        BEQZ R3, NOMAX2
        DADD R8, R1, R0

NOMAX2: DADDI R2, R2, #8
        DADDI R4, R4, #2
        SLT R5, R4, R9
        BNEZ R5, LOOP
```

Instruction Schedule for Dynamic Issue (in-order)



⑥

Ex: Issue Rules - 2 per cycle, at most 1 LD/SD, at most 1 float
 Latency: LD-2, int-1, F*-3, F+-3

LOOP: L.D F0, (R1)
 L.D F2, (R2)
 L.D F4, 8(R1)
 L.D F6, 8(R2)
 DADDI R1, R1, #16
 DADDI R2, R2, #16
 MUL.D F8, F0, F2
 MUL.D F10, F4, F6
 ADD.D F12, F8, F16
 ADD.D F14, F10, F16
 S.D F12, (R3)
 S.D F14, 8(R3)
 DADDI R3, R3, #16
 DADDI R4, R4, #2
 SLT R5, R4, R6
 BNEZ R5, LOOP

1	L.D F0, (R1)	-
2	L.D F2, (R2)	-
3	L.D F4, 8(R1)	-
4	L.D F6, 8(R2)	DADDI R1, R1, #16
5	DADDI R2, R2, #16	MUL.D F8, F0, F2
6	MUL.D F10, F4, F6	-
7	-	-
8	ADD.D F12, F8, F16	-
9	ADD.D F14, F10, F16	-
10	-	-
11	S.D F12, (R3)	-
12	S.D F14, 8(R3)	DADDI R3, R3, #16
13	DADDI R4, R4, #2	-
14	SLT R5, R4, R6	-
15	BNEZ R5, LOOP	-

16 instructions \Rightarrow 15 cycles

Instruction Schedule for Dynamic Issue (in-order)

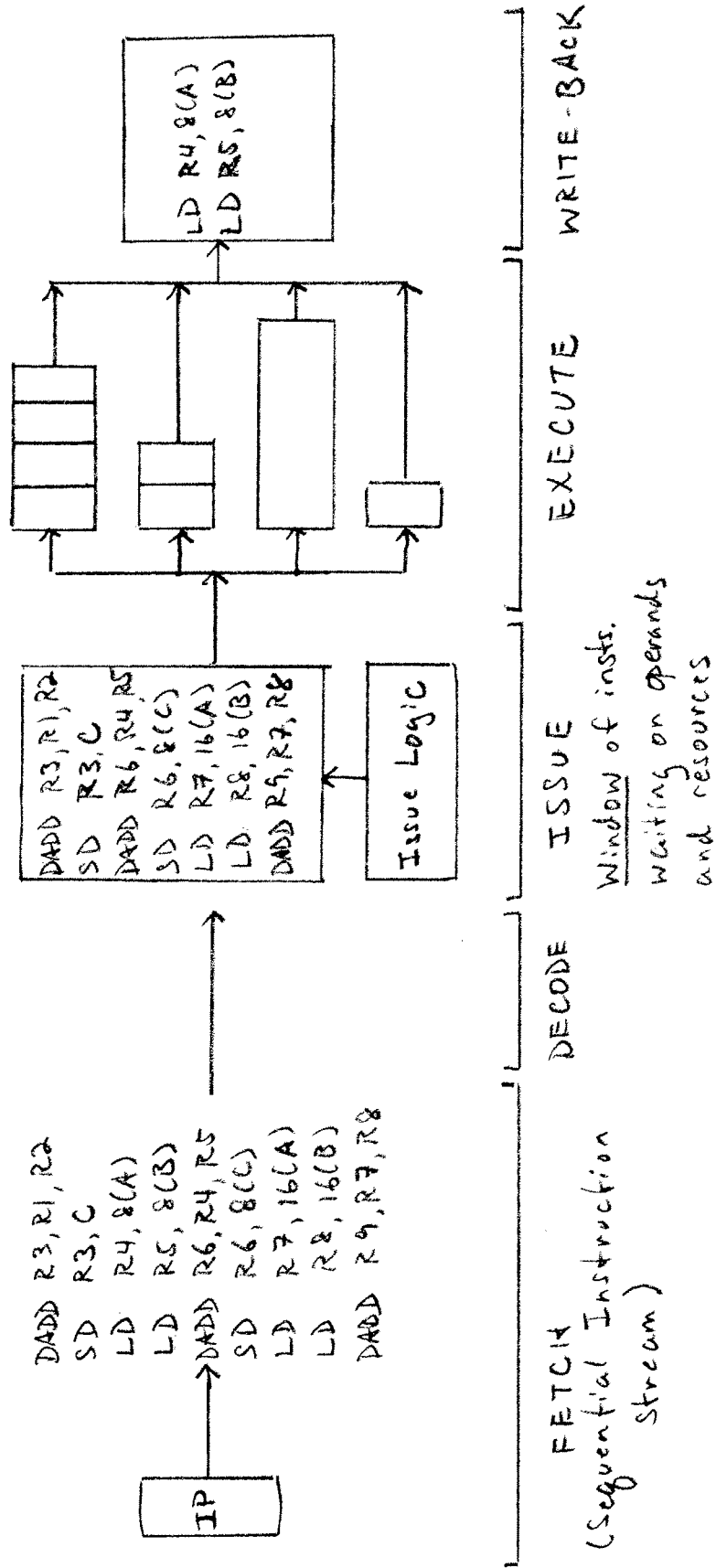
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Ex: Issue Rules - 2 per cycle, at most 1 LD/SD, at most 1 float
Latency: LD - 1, int - 0, F* - 2, F+ - 2

LOOP: L.D F0, (R1)	1 L.D F0, (R1)	DADDI R1, R1, #16
DADDI R1, R1, #16	2 L.D F2, (R2)	DADDI R2, R2, #16
L.D F2, (R2)	3 L.D F4, -8(R1)	DADDI R4, R4, #2
DADDI R2, R2, #16	4 L.D F6, -8(R2)	MUL.D F8, F0, F2
L.D F4, -8(R1)	5 DADDI R3, R3, #16	-
DADDI R4, R4, #2	6 SLT R5, R4, R6	MUL.D F10, F4, F6
L.D F6, -8(R2)	7 ADD.D F12, F8, F6	-
MUL.D F8, F0, F2	8 -	-
DADDI R3, R3, #16	9 ADD.D F14, F10, F16	-
MUL.D F10, F4, F6	10 S.D F12, -16(R3)	-
SLT R5, R4, R6	11 -	-
ADD.D F12, F8, F6	12 S.D F14, -8(R3) BNEZ R5, LOOP	
ADD.D F14, F10, F16		
S.D F12, -16(R3)		
S.D F14, -8(R3)		
BNEZ R5, LOOP		

16 instructions \Rightarrow 12 cycles

Dynamic Instruction Scheduling: Basic Idea



Static Instruction Scheduling

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
	F	D	I	E	M	W	-	E	E	E	E	W																		
①	L.D	F0,	A(R1)																											
②	L.D	F2,	B(R1)																											
③	MUL.D	F4,	F0,	F2																										
④	ADD.D	F6,	F4,	F8																										
⑤	S.D	F6,	D(R1)																											
⑥	DADDI	R1,	R1,	#8																										
⑦	SLT	R3,	R1,	R2																										
⑧	BNEZ	R3,	LOOP																											
⑨	L.D	F0,	A(R1)																											
⑩	L.D	F2,	B(R1)																											
⑪	MUL.D	F4,	F0,	F2																										
⑫	ADD.D	F6,	F4,	F8																										
⑬	S.D	F6,	D(R1)																											
⑭	DADDI	R1,	R1,	#8																										
⑮	SLT	R3,	R1,	R2																										
⑯	BNEZ	R3,	LOOP																											

Iteration i

Iteration i+1

for ($i=0; i < n; i++$) {
 $D[i] = A[i] \cdot B[i] + C;$
 $i \rightarrow R1, C \rightarrow F8, n \cdot 8 \rightarrow R2$
}

MUL.D - 3 cycles
ADD.D - 3 cycles

Dynamic Instruction Scheduling

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
① L.D F0, A(R1)	F	D	I	E	M	W																								
② L.D F2, B(R1)	F	D	I	E	M	W																								
③ MUL.D F4, F0, F2	F	D	I	E	M	W																								
④ ADD.D F6, F4, F8	F	D	I	E	M	W																								
⑤ S.D F6, D(R1)	F	D	I	E	M	W																								
⑥ DADDI R1, R1, #8	complete overlap																													
⑦ SLT R3, R1, R2																														
⑧ BNEZ R3, LOOP																														
⑨ L.D F0, A(R1)																														
⑩ L.D F2, B(R1)																														
⑪ MUL.D F4, F0, F2																														
⑫ ADD.D F6, F4, F8																														
⑬ S.D F6, D(R1)																														
⑭ DADDI R1, R1, #8																														
⑮ SLT R3, R1, R2																														
⑯ BNEZ R3, LOOP																														

iteration i

iteration i+1

for ($i=0; i < n; i++$) {
 $D[i] = A[i] \cdot B[i] + C;$
 $i \rightarrow R1, C \rightarrow F8, n-8 \rightarrow R2$
}

MUL.D - 3 cycles
ADD.D - 3 cycles