Scoreboarding Ex

```
                  1 2 3 4 5 6 7 8 9 10|11 12 13 14 15|16 17 18 19 20|21 22 ... 55 56 57
L.D F6, 34(R2)    F D I E M W
L.D F2, 45(R3)      F D I E M W
MUL.D F0, F2, F4      F D I - E E E E|E E E E E|E W
SUB.D F8, F6, F2        F D I - E E W
DIV.D F10, F0, F6         F D I - - -|- - - - - E E E E|E E ... E E W
ADD.D F6, F8, F2            F D I - E|E - - - - - - W
```

MUL.D - 9 cycles; DIV.D - 39 cycles; ADD.D, SUB.D - 1 cycle

cycle 8:

Busy bits:

F0	F2	F4	F6	F8	F10
1	0	0	0	1	1

	OPCODE	R_1	SR_1	R_2	SR_2	DR
ADD0	SUB.D	1	F6	1	F2	F8
ADD1						
MULT	MUL.D	1	F2	1	F4	F0
DIV	DIV.D	0	F0	1	F6	F10

Set busy bits [F6] = 1
allocate ADD1
  OPCODE ← ADD.D
  R_1 ← 0
  SR_1 ← F8
  R_2 ← 1
  SR_2 ← F2
  DR ← F6

cycle 10:

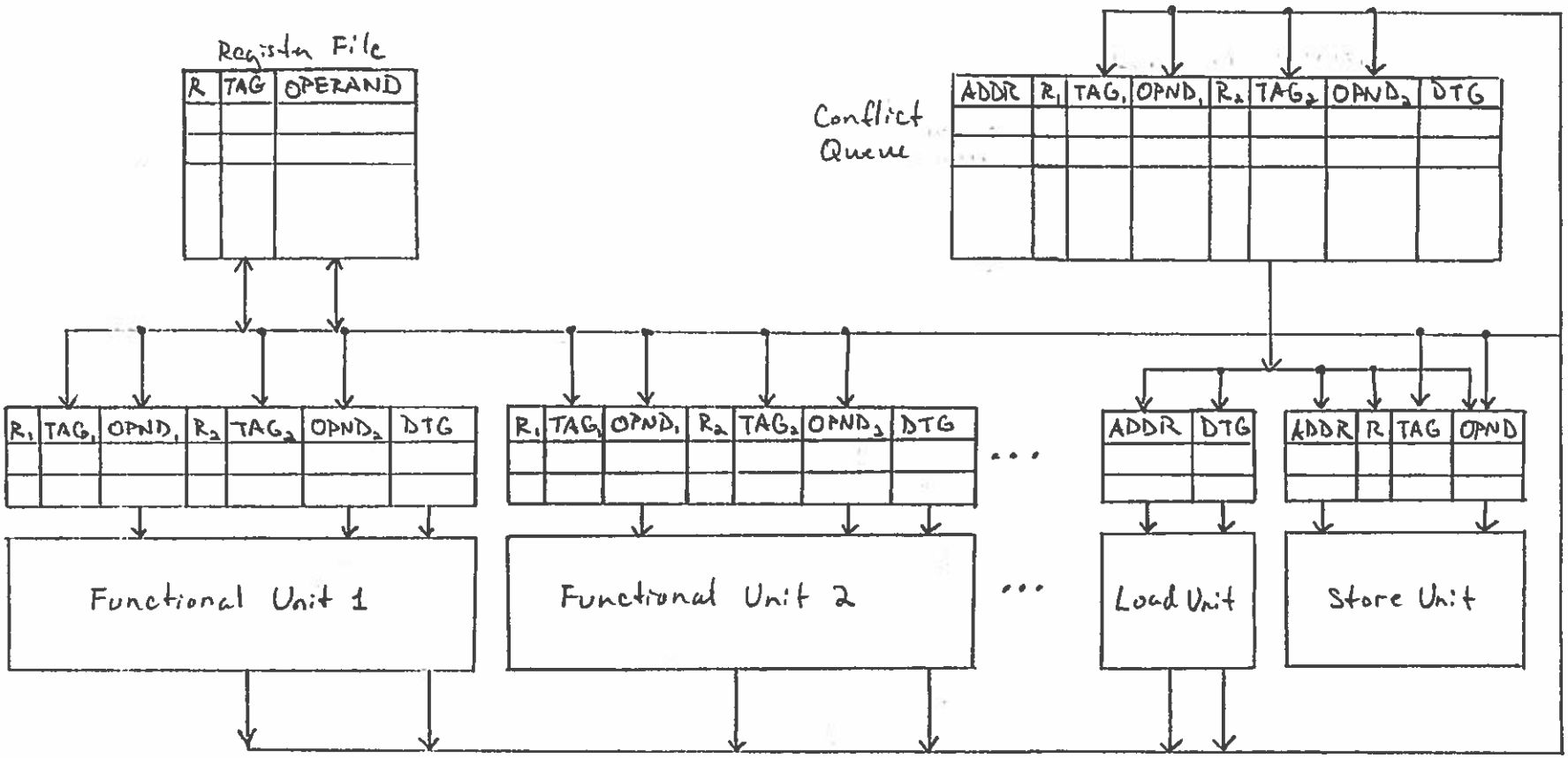
Busy bits:

F0	F2	F4	F6	F8	F10
1	0	0	1	1	1

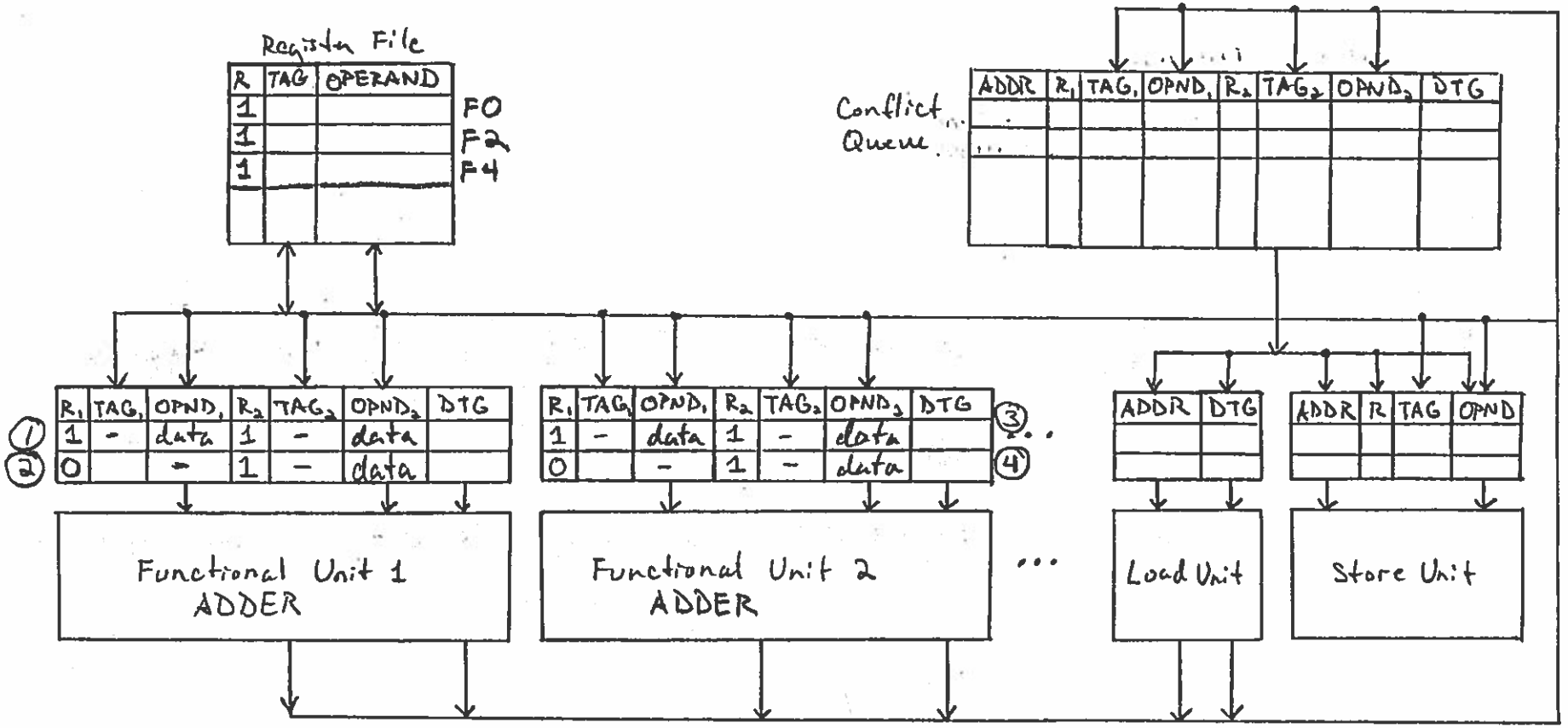
	OPCODE	R_1	SR_1	R_2	SR_2	DR
ADD0	SUB.D	1	F6	1	F2	F8
ADD1	ADD.D	0	F8	1	F2	F6
MULT	MUL.D	1	F2	1	F4	F0
DIV	DIV.D	0	F0	1	F6	F10

Write Result → REG[F8]
Reset busy bits [F8] = 0
Deallocate ADD0
Check scoreboard
  match waiting source and F8 for ADD1
  set ADD1.R_1 = 1
Issue ADD1

Dynamic Scheduling Using Reservation Stations
(Tomasulo's Algorithm)



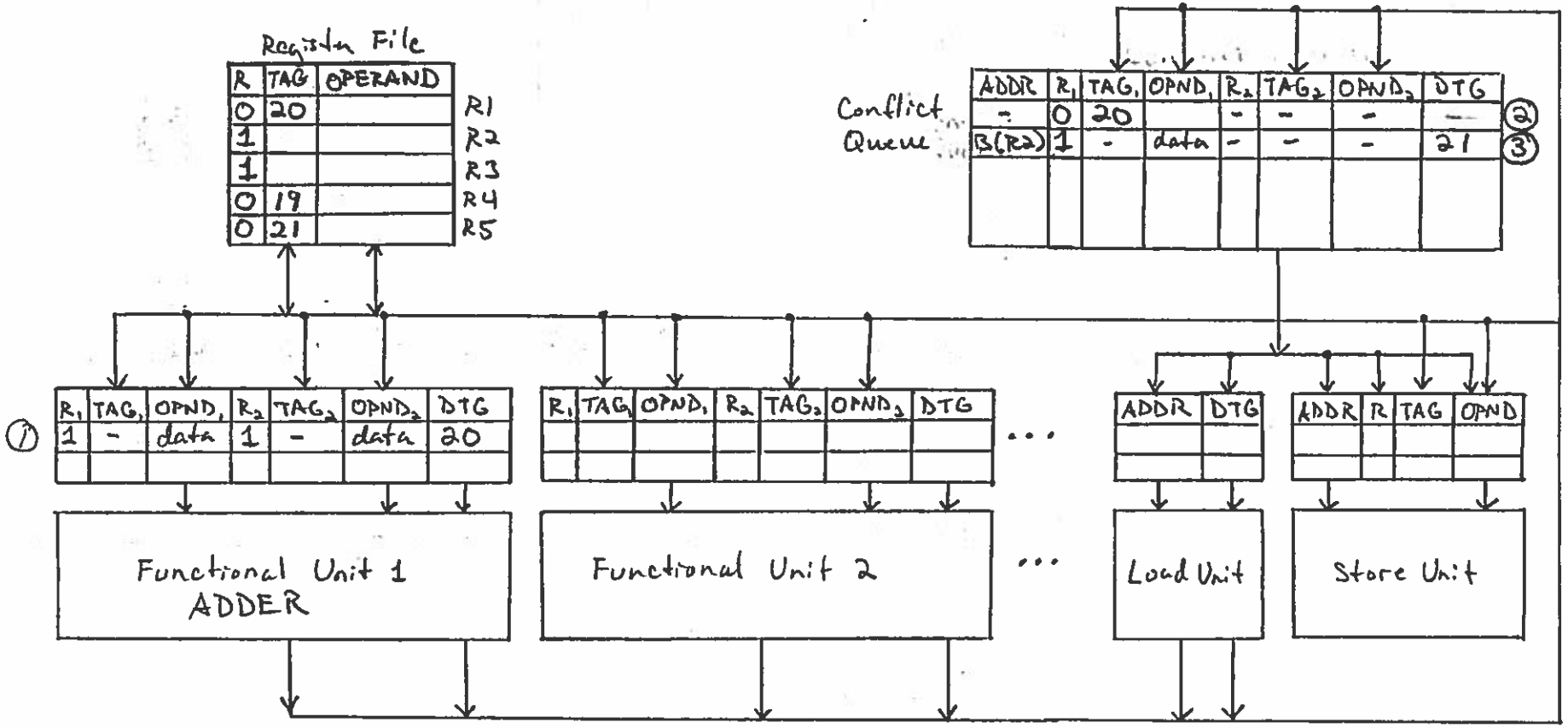
Dynamic Scheduling Using Reservation Stations
(Tomasulo's Algorithm)



Register Renaming Example

① ADD F0 F4 F4
② ADD F2 F0 F4
③ ADD F0 F4 F4
④ ADD F2 F0 F4

Dynamic Scheduling Using Reservation Stations
(Tomasulo's Algorithm)



Memory Disambiguation Example

① ADD R1 R2 R3
② SW R4 A(R1)
③ LW R5 B(R2)

Tomasulo's Algorithm Example

		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
iteration i	① L.D F0, A(R1)	F	D	I	E	M	W																								
	② L.D F2, B(R1)		F	D	I	E	M	W																							
	③ MUL.D F4, F0, F2			F	D	I	-	E	E	E	E	E	E	E	E	E	E	W													
	④ ADD.D F6, F4, F8				F	D	I	-	-	-	-	-	-	-	-	-	-	E	E	E	E	W									
	⑤ S.D F6, D(R1)					F	D	I	(E)	-	-	-	-	-	-	-	-	-	-	-	-	E	M	W							
	⑥ DADDI R1, R1, #8						F	D	I	E	M	W																			
	⑦ SLT R3, R1, R2							F	D	I	E	M	W																		
	⑧ BNEZ R3, LOOP								F	D	I	E	M	W																	
iteration i+1	⑨ L.D F0, A(R1)									-	-	-	F	D	I	E	M	W													
	⑩ L.D F2, B(R1)												F	D	I	E	M	W													
	⑪ MUL.D F4, F0, F2													F	D	I	E	M	W												
	⑫ ADD.D F6, F4, F8														F	D	I	-	E	E	E	E	E	E	E	E	E	E	W		
	⑬ S.D F6, D(R1)																F	D	I	(E)	-	-	-	-	-	-	-	-	-	E	
	⑭ DADDI R1, R1, #8																	F	D	I	E	M	W								
	⑮ SLT R3, R1, R2																		F	D	I	E	M	W							
	⑯ BNEZ R3, LOOP																			F	D	I	E	M	W						

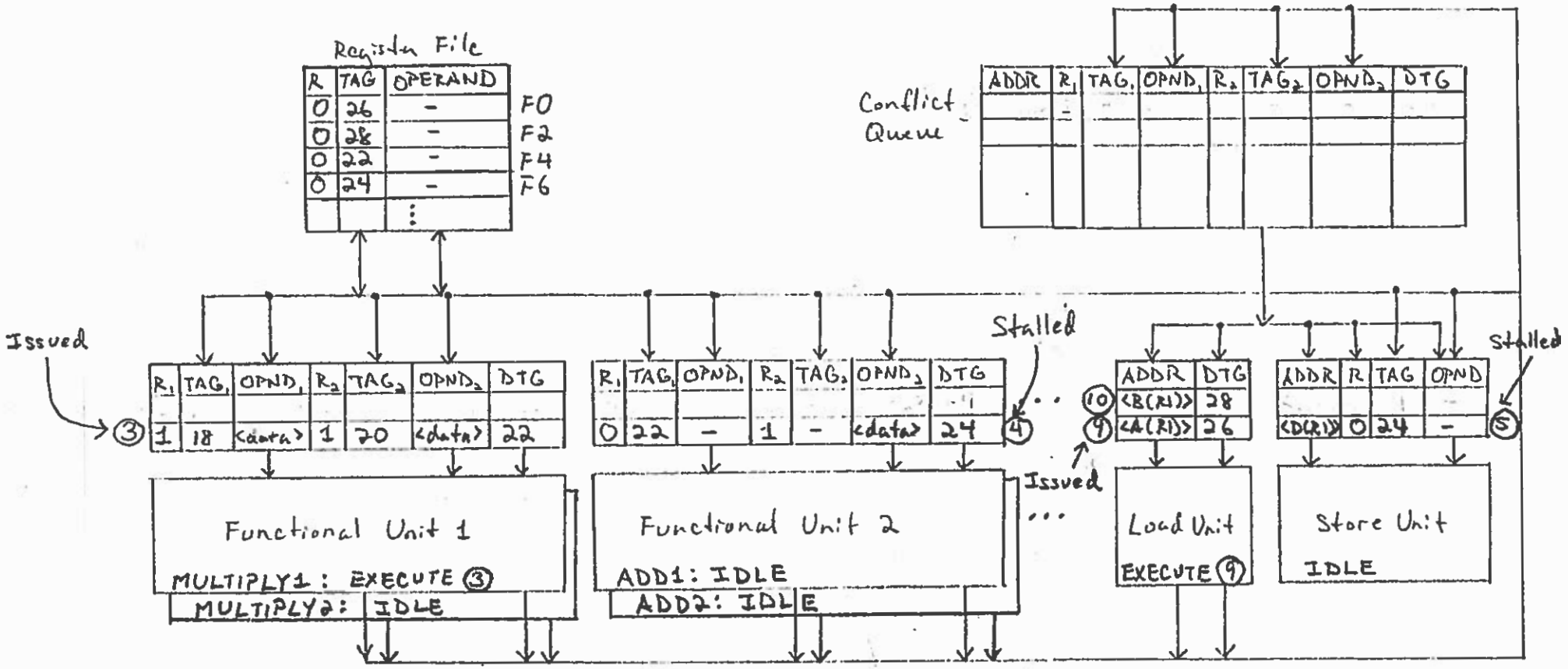
```
for( i=0; i<n; i++){
    D[i] = A[i] · B[i] + C;
}
```

i → R1, C → F8, n·8 → R2

MUL.D - 9 cycles
ADD.D - 3 cycles

UT

Dynamic Scheduling Using Reservation Stations
(Tomasulo's Algorithm)

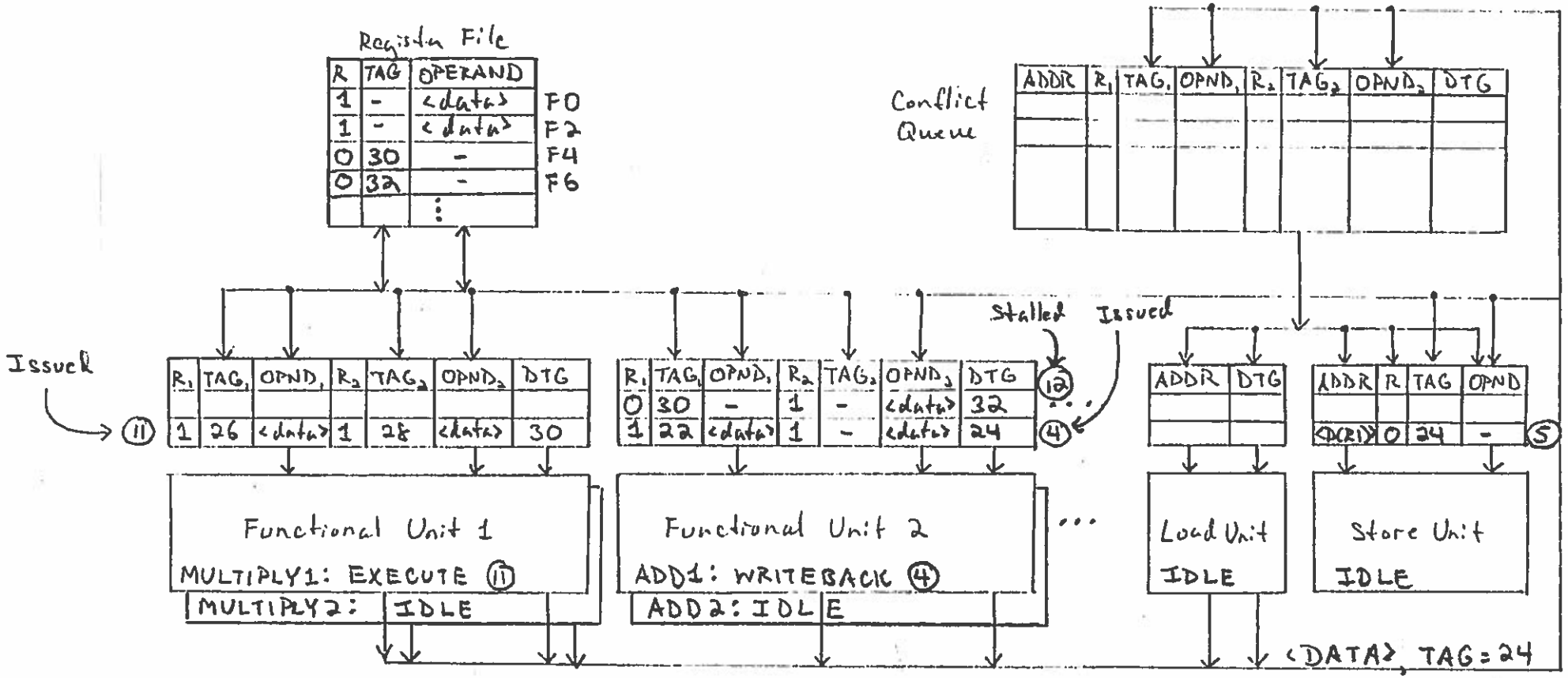


Cycle 16: Issue MULTD (instruction 11)

Rename F0 → 26
Rename F2 → 28
Rename F4 → 30

$R_1 = 0$
$TAG_1 = 26$
$OPND_1 = -$
$R_2 = 0$
$TAG_2 = 28$
$OPND_2 = -$
DTG = 30

Dynamic Scheduling Using Reservation Stations
(Tomasulo's Algorithm)



Cycle 21: ADDD Completes (Instruction ④)

Assert <DATA>, TAG=24 onto result bus

TAG matches instruction ⑤ in store unit

TAG <u>does not</u> match in register file