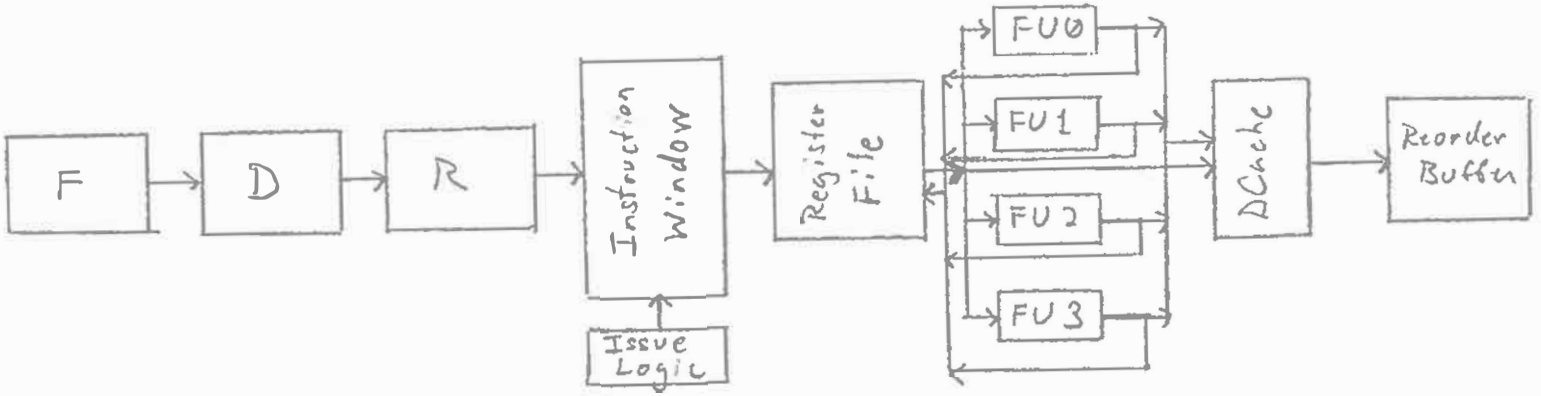
Modern Superscalar Case Study

from Palacharla, Jouppi, + Smith - ISCA '97

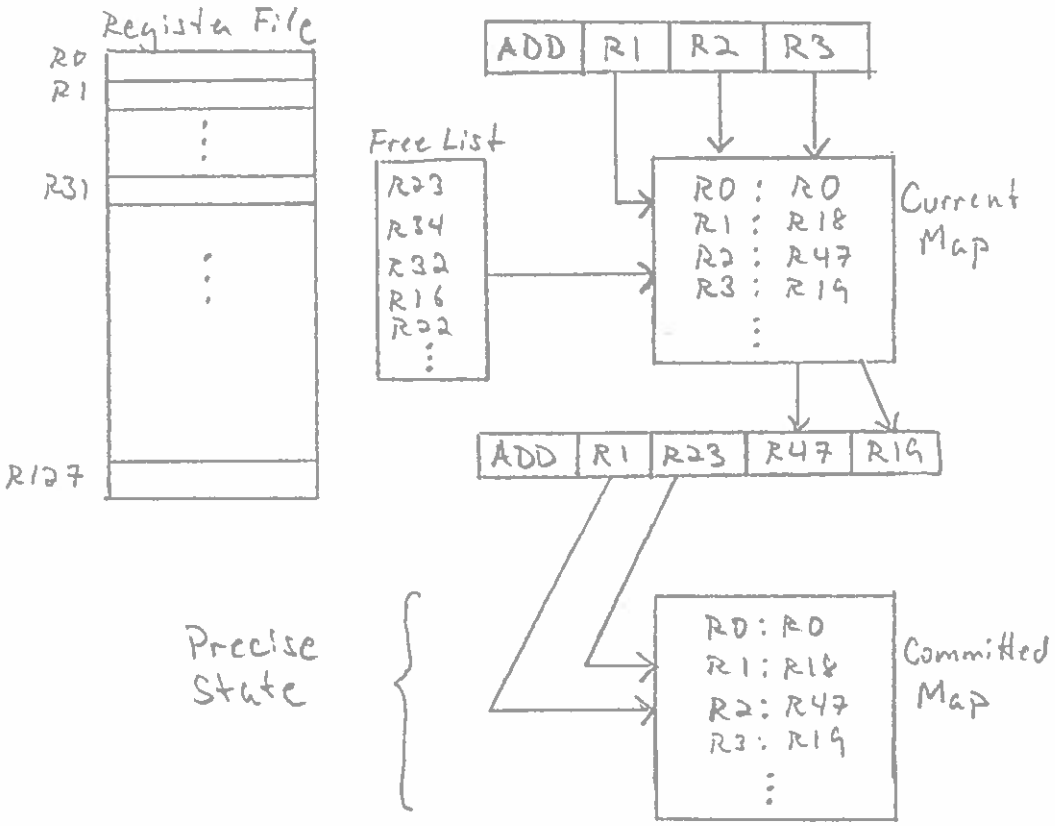


Fetch Decode Rename Issue Regstn Read Execute Memory Commit

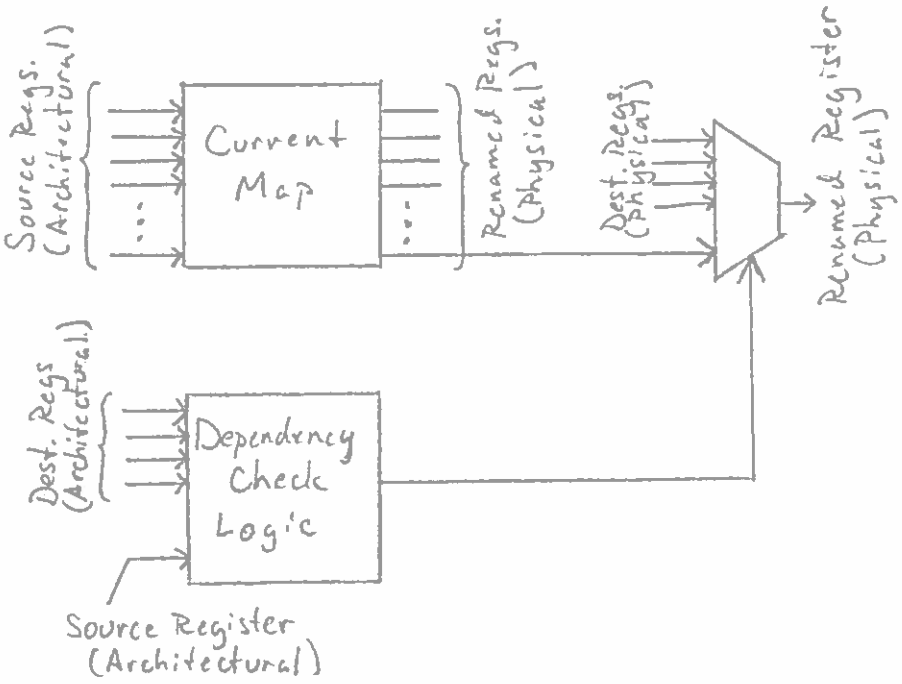
Example Pipeline (Similar to MIPS R10000, DEC 21264)

Register Renaming

Renaming 1 instruction:

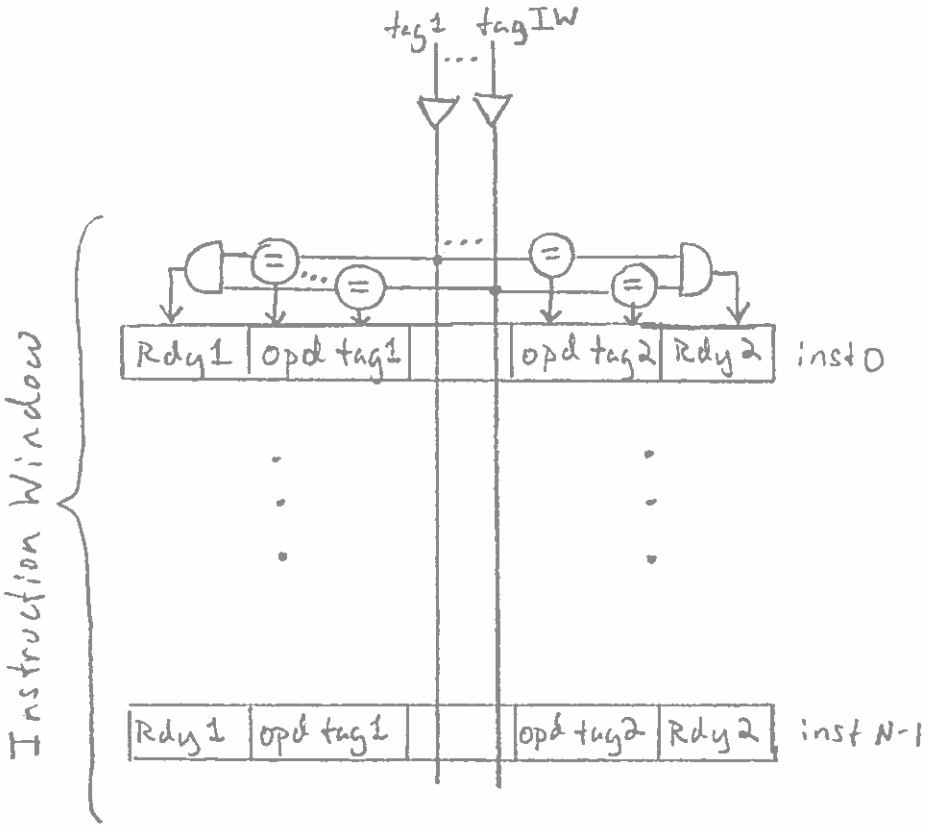


Renaming Multiple Instructions:

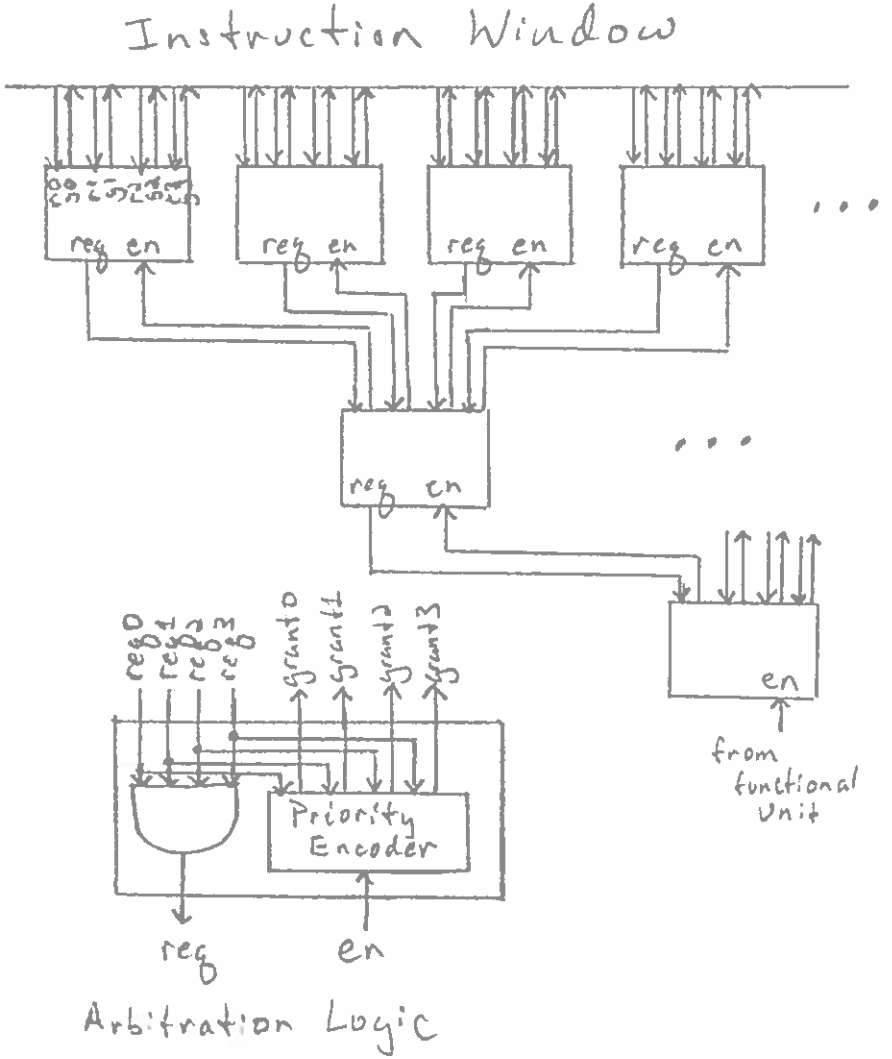


Issue

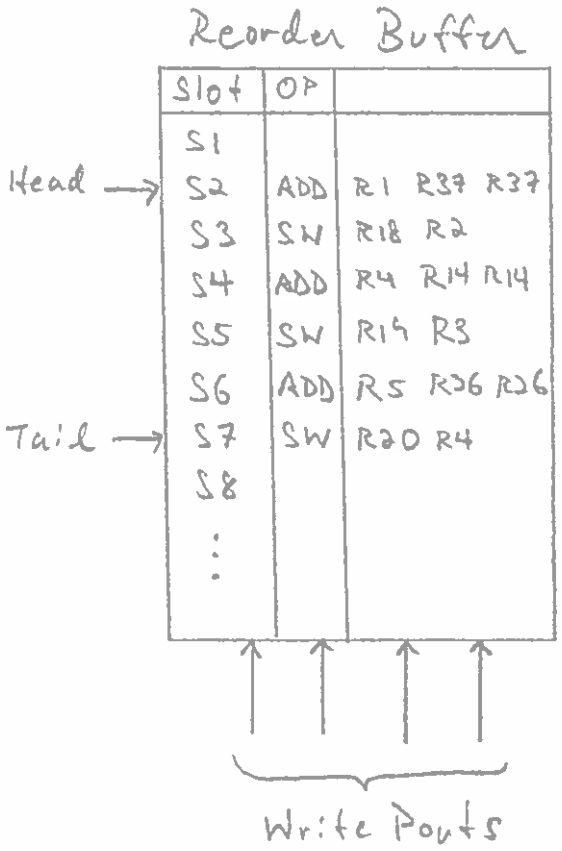
Wakeup Logic:



Select Logic:



Commit



- Commit instructions in-order.
  - Check exceptions
  - update Committed Map
  - update memory
- Maintain slots as a circular buffer
  - Commit instructions from head.
  - Allocate slots from tail.