ENEE 446: Digital Computer Design

Fall 2018 **Handout #6**

Problem Set # 1 Due: Sept. 12

Computer Architecture Basics

Problem 1

H&P 1.8

Problem 2

H&P 1.15

Problem 3

Suppose we are considering a change to an instruction set. The base machine initially has only loads and stores to memory, and all operations work on the registers. Such machines are called *load-store* machines. Measurements of the load-store machine showing the *instruction mix* and clock cycle counts per instruction are given as follows:

Instruction type	Frequency	Clock cycle count
ALU ops	43%	1
Loads	21%	2
Stores	12%	2
Branches	24%	2

Let's assume that 25% of the *arithmetic logic unit* (ALU) operations directly use a loaded operand that is not used again.

We propose adding ALU instructions that have one source operand in memory. These new *register-memory instructions* have a clock cycle count of 2. Suppose that the extended instruction set increases the clock cycle count for branches by 1, but it does not affect the clock cycle time. Would this change improve CPU performance?

Problem 4

H&P C.1, parts a. through e.