ENEE 446: Digital Computer Design

Fall 2018 **Handout #1**

Course Information and Policy

Room:	EGR 0108 MW 2:00p.m. - 3:15p.m.
Web:	http://www.ece.umd.edu/class/enee446.F2018
Instructor:	Donald Yeung 1323 A. V. Williams (301) 405-3649 yeung@eng.umd.edu http://www.ece.umd.edu/~yeung
Office Hours:	MW 3:30-4:30
TAs:	Dylan O'Reagan and Chenxi Wen oreagandylan@gmail.com and sunnywen441@gmail.com

1 Goal

In this course, you will obtain an in-depth understanding for how modern computers are organized, and why they are organized that way. Core topics of the course include pipelining, exploiting instruction-level parallelism, caching and virtual memory, multicore processors, techniques for power efficiency, and I/O systems.

2 Text

Hennessy and Patterson. *Computer Architecture: A Quantitative Approach*, 5^{th} Edition.

3 Prerequisites

The course prerequisite is ENEE 350, or equivalent. Students should understand basic computer organization, logic design, and assembly language programming. Also, it is important for students to be familiar with a high-level programming language, such as C. The programming assignments will require students to write a fair amount of code. Questions concerning background should be brought up with the instructor.

4 Assignments

There will be 4-5 problem sets and two programming assignments. All assignments will be handed out in class.

Late Problem Sets

Each problem set handout will indicate a due date at the top of the handout. Problem sets will be due in class on that date. No late problem sets will be accepted.

Collaboration

Students are encouraged to work together on problem sets, **but each student must hand in his/her own solutions**. Also, no more than three students can work on a problem set together, and each student should indicate the names of all group members at the top of his/her problem set. Students may discuss the programming assignments with each other, but each student must design, implement, and hand in his/her own code.

5 Exams

There will be one midterm, and one final exam. The dates of the exams are indicated (tentatively) on the course schedule.

6 Grading

A student's grade will be determined by his/her performance on the problem sets, programming assignments, midterm, and final exam according to the following breakdown:

Problem sets	15%
Programming	15% (each)
Midterm	20%
Final exam	35%

7 Honor Code

You are responsible for upholding the policies on collaboration and team work on the problem sets and programming assignments. In particular, copying solutions to either the problem sets or programming assignments from **any source** is prohibited.

8 Class Web Page

The class web page is located at http://www.ece.umd.edu/class/enee446.F2018. All handouts, problem sets, programming assignments, and solutions will be posted on this page after they have been distributed in class. Also, a course schedule will be posted and will reflect all changes in the lecture content, assignments, and exam schedules.

9 Course Schedule

In the remainder of this handout, you will find a tentative course schedule. Check the class web page for revisions to the schedule as the semester progresses.

Lecture	Date	Topic	Reading	Out	In
1	27 Aug	Welcome to ENEE 446 Introduction: What is computer architecture?	H&P 1.1 - 1.12		
2	29 Aug	Pipelining I: Review of basic concepts	H&P C.1 - C.3	HW 1	
3	5 Sep	Pipelining II: Exceptions	H&P C.4 - C.6		
4	10 Sep	Pipelining III: Multi-cycle operations			
5	12 Sep	Instruction-Level Parallelism I: Introduction to ILP	H&P 3.1 - 3.2, 3.10		HW 1
6	17 Sep	Instruction-Level Parallelism II: Multiple issue machines	H&P 3.7	PR 1	
7	19 Sep	Instruction-Level Parallelism III: Dynamic instruction scheduling	H&P 3.4		
8	24 Sep	Instruction-Level Parallelism IV: Scoreboarding	H&P C.7 - C.10		
9	26 Sep	Instruction-Level Parallelism V: Tomasulo's Algorithm	H&P 3.5		
10	1 Oct	Instruction-Level Parallelism VI: Dynamic branch prediction	H&P 3.3, 3.6, 3.9	HW 2	PR 1
11	3 Oct	Caching I: Cache organizations	H&P B.1, 2.1		
12	8 Oct	Caching II: Cache performance optimizations	H&P B.2 - B.3, 2.2		
13	10 Oct	slack			HW 2
EXAM	15 Oct	Midterm			

Lecture	Date	Topic	Reading	Out	In
14	17 Oct	Caching III: Cache performance optimizations			
15	22 Oct	Multicore I: Parallel Programming Models	H&P 5.1	HW 3	
16	24 Oct	Multicore II: Snoopy Cache Coherence	H&P 5.2 - 5.3		
17	29 Oct	Multicore III: Directory-based Cache Coherence	H&P 5.4		
18	31 Oct	Multicore IV: Memory Consistency Models	H&P 5.6		HW 3
19	5 Nov	Power I: Modeling		PR 2	
20	7 Nov	Power II: Low-Power Techniques			
21	12 Nov	Power III: Low-Power Techniques			
22	14 Nov	Virtual Memory I: Naming and protection	H&P B.4 - B.5, 2.4		
23	19 Nov	Virtual Memory II: Resource management			PR 2
24	26 Nov	Virtual Memory III: Resource management		HW 4	
25	28 Nov	Main Memory	H&P 2.3		
26	3 Dec	I/O I: I/O devices			
27	5 Dec	I/O II: Basic I/O architecture			HW 4
28	10 Dec	slack			
EXAM	15 Dec 1:30-3:30	FINAL			