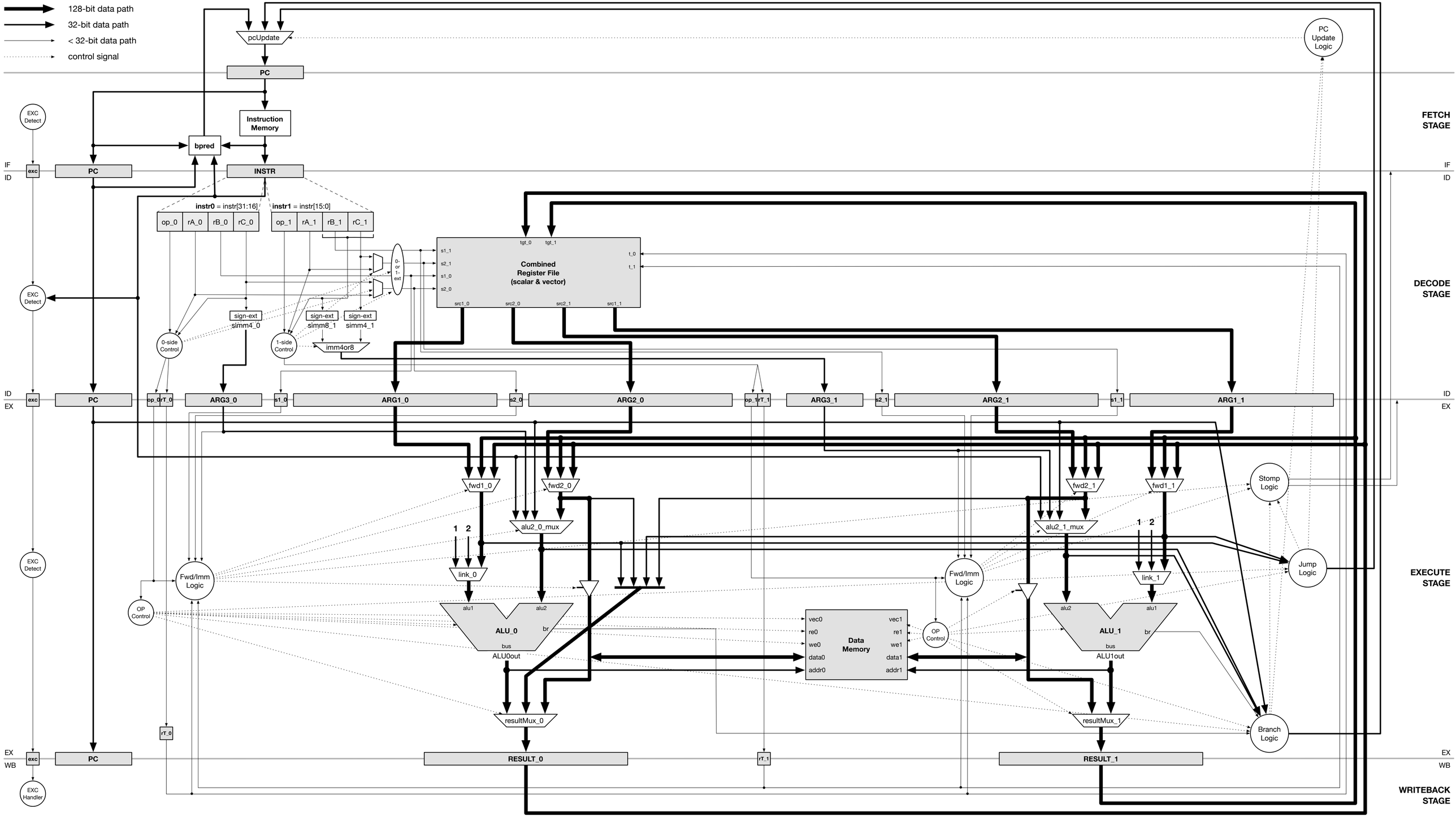
128-bit data path
32-bit data path
< 32-bit data path
control signal
pcUpdate
PC
PC Update Logic
Instruction Memory
bpred
EXC Detect
exc
PC
INSTR
IF
ID
FETCH STAGE
instr0 = instr[31:16]
instr1 = instr[15:0]
op_0
rA_0
rB_0
rC_0
op_1
rA_1
rB_1
rC_1
0- or 1- ext
Combined Register File (scalar & vector)
tgt_0
tgt_1
s1_1
s2_1
s1_0
s2_0
t_0
t_1
src1_0
src2_0
src2_1
src1_1
DECODE STAGE
sign-ext
simm4_0
simm8_1
simm4_1
imm4or8
0-side Control
1-side Control
EX
op_0
rT_0
ARG3_0
s1_0
ARG1_0
s2_0
ARG2_0
op_1
rT_1
ARG3_1
s2_1
ARG2_1
s1_1
ARG1_1
fwd1_0
fwd2_0
fwd2_1
fwd1_1
Stomp Logic
alu2_0_mux
alu2_1_mux
1
2
link_0
link_1
Jump Logic
Fwd/Imm Logic
OP Control
alu1
alu2
ALU_0
br
bus
ALU0out
ALU_1
ALU1out
vec0
re0
we0
data0
addr0
Data Memory
vec1
re1
we1
data1
addr1
resultMux_0
resultMux_1
Branch Logic
EXECUTE STAGE
rT_0
rT_1
WB
RESULT_0
RESULT_1
EXC Handler
WRITEBACK STAGE