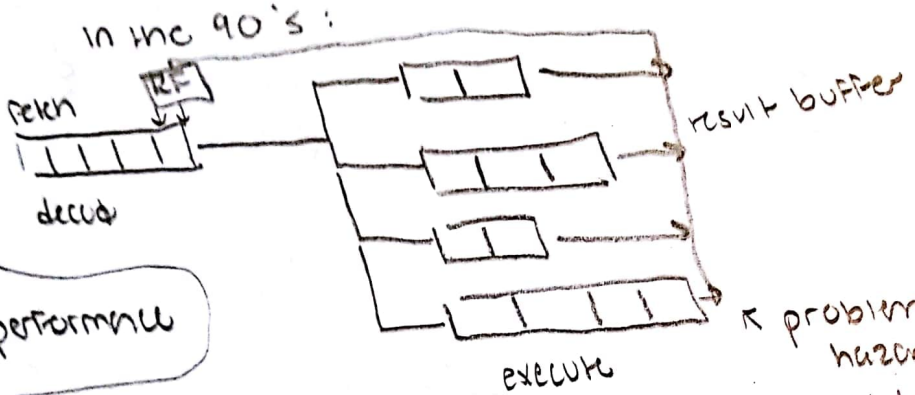
1. Discuss the technique of **PIPELINING** a processor design. What are the **tricky implementation issues**? What is the effect of pipelining on processor performance? (support your answer quantitatively)

5/5

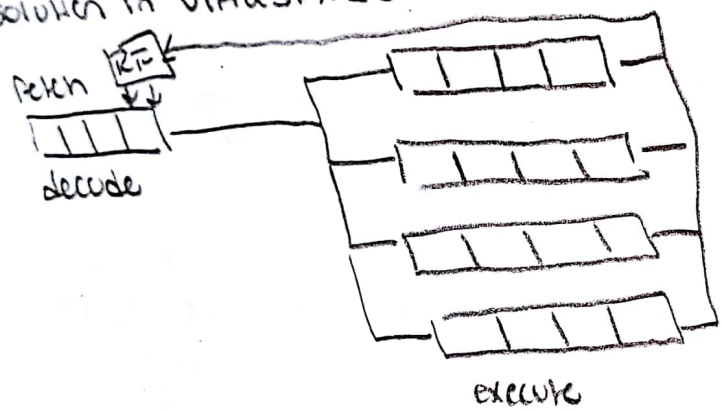
In the 90's:



pipeline is a cheap way to get good performance

↖ problem: structural hazard, multiple things may try to write to this buffer at once

solution in UltraSPARC



now execute takes some amount of time for every instruction

Pipelines allow multiple instructions to be processed at once by dividing them up into stages (fetch, decode, execute, writeback)

↳ there is also sometimes a separate stage for memory

Important note: instructions DO NOT get executed faster, but more instructions are completed per cycle (better performance?)

ex. instead of

time →	1	2	3	4	5	6
instr 1	F	D	X	W		
instr 2					F	D X W

. at cyc 6, only 1 full instruction has been completed

a pipeline allows for

time →	1	2	3	4	5	6
instr 1	F	D	X	W		
instr 2		F	D	X	W	
instr 3			F	D	X	W
instr 4				F	D	...
instr 5					F	

at cyc 6, 2 full instructions have been completed