tricky implementation issues:

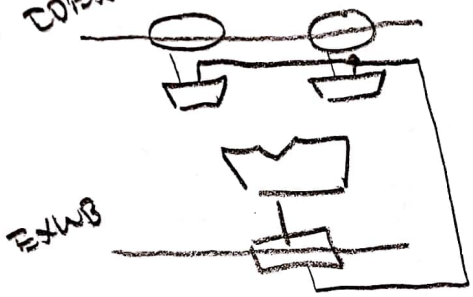
data hazards: this occurs when instructions rely on each others data but it may not be available yet

solutions: 0. define not a problem / change architecture

1. stall until data is ready (use valid signals from SRAM)

2. use data forwarding

ex. IDEX



or

IDEX

control hazards: when there is a conditional branch or jump

if branch executes early, make sure these aren't effected

solutions: 0. define not a problem

1. stall

2. conditional instructions

ex. [ ] lw

↑ only execute if this condition is true

3. branch prediction