Memory Transaction

Single Memory Access:

Ex: \[ t_{\text{address}} = 10\,\text{ns} \]
\[ t_{\text{data-access}} = 50\,\text{ns} \]
\[ t_{\text{data-transfer}} = 10\,\text{ns} \]

Total access latency = 70ns

Interleaved Memory Access:

<table>
<thead>
<tr>
<th>Address</th>
<th>Bus</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADDR1</td>
<td></td>
</tr>
<tr>
<td>ADDR2</td>
<td></td>
</tr>
</tbody>
</table>

Bank 0:

Data Access

Bank 1:

Data Access

Data Bus:

Data1      | Data2
Low Order Interleaving

How many banks are needed?

Address:

Bus:

A1 A2 A3 A4 A5 A6 A7 ...

Bank 0:

Bank 1:

Bank 2:

Bank 3:

Bank 4:

Bank 5:

Data Bus:

D1 D2 D3 D4 D5 D6 D7
DRAM Architecture

EDO DRAM:

- DRAM page size typically the square root of DRAM size
  - e.g., 64 Mbit DRAM $\Rightarrow$ 8 Kbits $= 1$ Kbytes
  - lots of data in a DRAM page

```
Address:  \[\text{ROW} \quad \text{COL1} \quad \text{COL2} \quad \text{COL3} \quad \ldots\]
```

```
Data:  \[\text{Data } 1 \quad \text{Data } 2 \quad \text{Data } 3 \quad \ldots\]
```
DRAM Architecture

Multiple internal banks:

Bank 0

Bank 1

Small SRAM Cache

I/O Pins

Row Decode

Column Decoder

Sense Amplifier

Row Decode

CDRAM:

DRAM Array

Row Decode