Modern Superscalar Case Study
from Palachanla, Jouppi, & Smith - ISCA '97

Fetch Decode Rename Issue Read Execute Memory Commit

Example Pipeline (Similar to MIPS R10000, DEC 21264)
Register Renaming

Renaming 1 instruction:

Renaming Multiple Instructions:

Precise State
Issue

Wake-up Logic:

Instruction Window

Select Logic:

Instruction Window

from functional Unit

Arbitration Logic
Commit

- Commit instructions in-order:
  - Check exceptions
  - Update Committed map
  - Update memory

- Maintain slots as a circular buffer
  - Commit instructions from head
  - Allocate slots from tail

Reorder Buffer

<table>
<thead>
<tr>
<th>Slot</th>
<th>OP</th>
</tr>
</thead>
<tbody>
<tr>
<td>S1</td>
<td>add</td>
</tr>
<tr>
<td>S2</td>
<td>sd</td>
</tr>
<tr>
<td>S3</td>
<td>sd</td>
</tr>
<tr>
<td>S4</td>
<td>add</td>
</tr>
<tr>
<td>S5</td>
<td>sd</td>
</tr>
<tr>
<td>S6</td>
<td>add</td>
</tr>
<tr>
<td>S7</td>
<td>sd</td>
</tr>
<tr>
<td>S8</td>
<td></td>
</tr>
</tbody>
</table>

Write Ports