ENEE 601 MID-TERM: 29 MARCH 2007

I. SEMICONDUCTOR PHYSICS (20Pts)

1. Changing the temperature affects the position of the Fermi level. Explain, verbally, why this happens and discuss the limiting cases of very high and very low temperature. 2. If the "bulk potential" (the separation of the Fermi level from mid-gap) is 0.35V and N_d is 10^{16}, what is the "doping efficiency" (the fraction of ionized donors). In class, we didn't talk about the "g"-factor (spin-degeneracy factor) much. But in calculating trap occupancies, it is an important constant. It shows up as the term "g" given on the formulary. For donor states, g=1/2. Please use it in this problem.

II. DIODES AND CONTACTS (20Pts)

1. We frequently find p+/p or n+/n layers in integrated circuits. These are used as Ohmic contacts. (a) What makes these structures work as Ohmic contacts (as opposed to blocking contacts)? Remember to consider the issue of work-function difference between the metal and bulk silicon in your discussion. (b) There is no "depletion" layer associated with these structures. What does the mobile electron and hole and fixed background charge distribution look like in these structures (e.g., are there internal fields? In which direction do they point?)

III. CAPACITORS (30Pts)

Consider the following capacitor structure: d_{ox}= 10nm, N_a (the silicon donor background) = 10^{16}. Assume that there are no "defect" charges in the oxide or at the oxide/semiconductor interface. Further assume that the work-function difference between the capacitor top plate and the bulk semiconductor is zero. (a) Draw the high and low-frequency CV plots you'd expect to obtain from this structure. Be careful to label (using real numbers) the positions and magnitudes of (b) C_{max}, C_{min} and C_{FB}. Now, suppose the field plate work function is 0.2 volts higher than the bulk semiconductor work function. (c) What does this do to the CV plot? PROVIDE NUMERICAL DESCRIPTIONS!

IV. TRANSISTORS (30Pts)

Consider a n-channel MOSFET with an 0.13 μm "as drawn" channel length. Take the S/D contacts to be doped to $10^{19}/cm^3$. Assume the maximum supply voltage is 3V (maximum voltage that can be applied to the gate or to the drain). Take the source as grounded. (a) What is the smallest channel doping that would insure that the drain space charge never touches the source space charge in the bulk of the silicon? (b) Ignoring work-function differences and oxide defect charge, what's the threshold voltage here?